

Current versus gate voltage hysteresis in organic field effect transistors

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Abstract Research into organic field effect transistors (OFETs) has made significant advances—both scientifically and technologically—during the last decade, and the first products will soon enter the market. Printed electronic circuits using organic resistors, diodes and transistors may become cheap alternatives to silicon-based systems, especially in large-area applications. A key parameter for device operation, besides long term stability, is the reproducibility of the current–voltage behavior, which may be affected by hysteresis phenomena. Hysteresis effects are often observed in organic transistors during sweeps of the gate voltage (V_{GS}). This hysteresis can originate in various ways, but comparative scientific investigations are rare and a comprehensive picture of “hysteresis phenomena” in OFETs is still missing. This review provides an overview of the physical effects that cause hysteresis and discusses the importance of such effects in OFETs in a comparative manner.

Keywords Organic thin-film transistors · Threshold voltage shift · Organic semiconductors · Organic dielectrics

Introduction

The first thin-film transistor (TFT) was reported in 1962 by Weimer [1]. The first reports on organic field effect

transistors (OFETs) using organic semiconductors on inorganic dielectrics appeared twenty years later [2–4]. Pioneering work towards all-organic OFETs that involved testing various organic dielectrics was done by Peng et al. [5]. Various examples of the applications of OFETs, such as large-area electronic applications, printed electronics, electronic paper (e-paper) [6], electronic skin, etc., are documented in [7]. For many applications, speed is not a limiting issue these days, since operation at up to 2 MHz has been demonstrated in OFET circuits [8]. Companies have presented printed logic circuits for RFID tags [9], a cell phone with an electrophoretic display addressed by an active matrix OFET backplane [10], and a backplane OFET array for e-paper [11].

The enormous interest in the field of OFETs [7, 12] is demonstrated by various scientific review articles published on charge transport [13, 14], on semiconductors for OFETs [15], on gate dielectrics [16, 17], on progress in plastic electronic devices [18] and on OFETs as sensors [19, 20]. In papers dealing with OFETs, statements like “hysteresis must be avoided” or “only negligible hysteresis is observed” can often be found. Hysteresis is a bistability in the operational transistor current. It appears as a difference in the source-drain current (I_{DS}) values observed during forward and backward sweeps of the gate voltage (V_{GS}). As such, it is not an unwanted feature per se—it could be useful in nonvolatile memory devices—but it must be avoided in standard integrated circuits.

Examples from inorganic transistors

Some of the mechanisms that cause hysteresis in OFETs are already quite well described in the literature on inorganic field effect transistor devices. Important hysteresis-related charge properties in silicon–silicon oxide

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MOS-FET transistors can also be found in OFETs, even if their descriptions are generally more complex in this context. In Si–SiO₂ systems, four general types of charge are known [21]:

1. *Interface-trapped charge* (also called surface state, interface state or fast state) are defects or impurities at the interface that can be charged or discharged.
2. *Fixed charge in oxide* is a positive charge due to structural defects close to the channel (2 nm) that does not communicate with the underlying Si.
3. *Trapped charge in oxide* are electrons or holes trapped in the bulk of the oxide. These traps can be introduced during device fabrication, or charge (electrons or holes) can be injected during device operation.
4. *Mobile charge in oxide* are mainly small alkali metal cations and H⁺, but can also be larger cations or anions (e.g., copper ions diffuse through germanium [22]). Flexodes (p–n junction devices with variable *I–V* characteristics resulting from reversible Li⁺ ion drift) were suggested in 1963 [23]. Mobile Na⁺ ions in SiO₂ gate dielectrics cause threshold voltage shifts in MOSFETs [24].

The occurrence of charges (1)–(4) in the Si–SiO₂ system leads to hysteresis phenomena in inorganic transistor devices. Interestingly, the practical application of Si MOSFETs was delayed in the early 1960s because of severe gate bias instability problems caused by mobile ionic charges like Na⁺, Li⁺, K⁺ and perhaps H⁺ [21]. Water is known to diffuse into SiO₂ that is not densely packed. A small amount dissociates into H⁺ and OH[–]. These ions can drift in an electric field to the channel and cause threshold voltage shifts [25].

Hysteresis phenomena have also been used as an advantage in field effect devices with a polarizable gate. The first ferroelectric field effect memory resistor was reported in 1963 [26], and the first field effect transistor with a ferroelectric gate in 1974 [27]. Problems with ferroelectric field effect memories (e.g., due to the depolarization field), as investigated in detail by Würfel et al. [28, 29], caused companies to leave this field. The revival of this field in the 1990s [30] brought ferroelectric memories onto the market [31, 32].

In most other cases besides memory applications, even a small degree of hysteresis is an unwanted effect. Its occurrence has been described in a number of publications. Hysteresis in a-Si TFTs increases with increasing temperature [33]. Leroux et al. [34] report that high-*k* dielectrics increase the number of traps and thereby the size of the hysteresis. In the silicon transistor literature, Fleetwood et al. [35] suggested distinguishing between the physical location of the defects (oxide traps, border traps and interface traps) and how such defects respond during the

measurement. Powell [36] termed the effects that are due to reversible trapping “dynamic V_{th} shift,” and the degradation effect “ V_{th} instability.” For references on investigations into bias stress effects in a-Si covering two decades, see Ref. [37].

Organic field effect transistors

Brown et al. [38] stated in 1997 that “hysteresis is noticeable by its absence in literature.” Recently, Mijalkovic [39] declared that memory effects (bias stress effects and hysteresis) are the biggest challenge in the modeling of OFETs and the corresponding circuit design. Threshold voltage shifts due to bias stress have been reported more frequently, but detailed investigations of these effects are rare, and a complete picture of the physical background that may cause hysteresis in OFETs is still missing.

In the following, a short introduction to OFETs, the characterization and measurement of hysteresis phenomena, and an overview of their physical background are presented. Significant papers that stress the different mechanisms that cause these bi- or instabilities are briefly discussed. The reported mechanisms are categorized below and are summarized in Fig. 1.

- (A) Effects of mobile charges at the channel [traps close to or in the channel (A1), charge injection from the semiconductor into the dielectric (A2), slow reactions of charge carriers in the organic semiconductor (A3), and mobile ions in the semiconductor (A4)]
- (B) Effects resulting in a polarization of the gate dielectric [ferroelectrics as dielectric or metastable

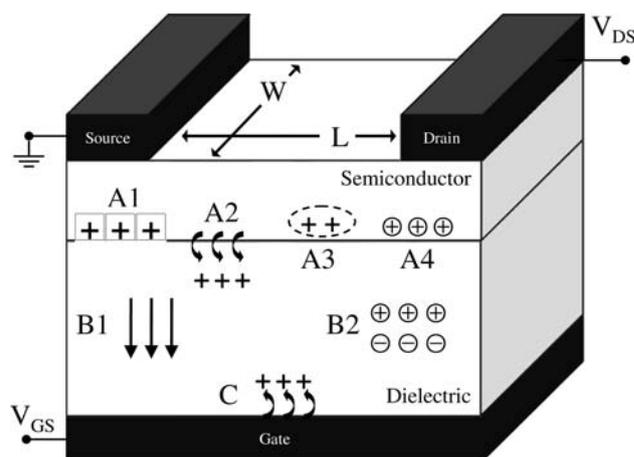


Fig. 1 Scheme of a staggered bottom gate OFET, illustrating the mechanisms that cause hysteresis. A detailed description of these mechanisms can be found in the text. In general, each effect is independent of the sign of the charge. For simplicity, only one type of charge is shown in the figure

- polarization in the dielectric (B1), and mobile ions in the dielectric (B2)]
- (C) Charge injection from the gate electrode into the dielectric

Introduction to OFETs

An OFET is a three-terminal device, as shown in Fig. 1. The current flows from the source electrode to the drain electrode, upon applying a voltage between the source and drain. This current can be influenced by a voltage applied to a third electrode (gate). Applying a voltage to the gate (V_{GS}) induces charges at the interface between the dielectric and the semiconductor. The layer of accumulated charges at the semiconductor/dielectric interface is called the channel. This channel enables high current flow between the source and drain (I_{DS}). The ratio between I_{DS} in the off state (no accumulation layer is present) and I_{DS} in the on state (an accumulation layer has formed) is called the on/off ratio, and this provides a measure of the performance of the OFET as an electronic switch. The conductive channel forms in a thin layer—a few nanometers thick [40]—at the semiconductor/dielectric interface. FETs are characterized by measuring transfer (I_{DS} vs. V_{GS}) and output (I_{DS} vs. V_{DS}) characteristics. A common model of field effect transistors [41] gives I_{DS} in the linear regime (at low V_{DS}) as:

$$I_{DS,lin} = W/L\mu_{FET}C_i(V_{GS} - V_{th})V_{DS}$$

The I_{DS} in the saturation regime (at high V_{DS}) is:

$$I_{DS,sat} = W/(2L)\mu_{FET}C_i(V_{GS} - V_{th})^2$$

W and L are the channel width and length, respectively (see Fig. 1). μ_{FET} is the field-effect mobility (of the majority charge carriers), C_i is the geometric capacitance of the dielectric, V_{GS} is the voltage applied to the gate, and V_{DS} is the voltage applied to the drain (both vs. the source, which is usually grounded). The charge carrier mobility is calculated in either the saturation or the linear regime from the above equations. In an ideal device, the mobilities calculated in the linear and saturation regimes are the same. The threshold voltage V_{th} can be extracted by determining the x axis intercept of $(I_{DS})^{1/2}$ versus V_{GS} in the saturation regime [42] or by the maximum of the second derivative of I_{DS} versus V_{GS} at low drain voltage [43]. The threshold voltage in the accumulation mode is given by [44]:

$$V_{th} = \pm qn_0d/C_i + V_{fb}$$

where V_{fb} is the flat-band potential, which accounts for any work-function difference between the semiconductor and the gate metal, q is the elementary charge, n_0 is the density

of free carriers, and d is the thickness of the semiconductor. The sign of the right-hand side in the equation corresponds to the sign of the charge carriers [44]. Based on this equation, a change in V_{th} between the forward scan and the reverse scan and thereby a hysteresis can be expected if: (1) n_0 changes (e.g., due to trapping of free charge carriers), (2) C_i changes (e.g., charge injection from the gate into the dielectric or polarization of the dielectric), and (3) V_{fb} changes (e.g., structural changes in the semiconductor).

Hysteresis

Cyclic transfer characteristics (I_{DS} vs. V_{GS}) where I_{DS} depends on the sweep direction of V_{GS} , are said to show “hysteresis,” as schematically depicted in Fig. 2. These reversible electrical bistabilities are frequently observed in organic field effect transistors. Depending on the microscopic effect, the hysteresis can result in a back sweep current (the sweep from on to off) that is either higher or lower than the forward sweep current (the sweep from off to on).

A hysteresis is sometimes described as turning “clockwise” or “anticlockwise.” However, these notations can be misleading, because the direction of the hysteresis also depends on the p- or n-type character of the investigated OFET, as demonstrated in Fig. 2.

Figure 2a and b show schematic transfer characteristics where the back sweep current is higher than the forward

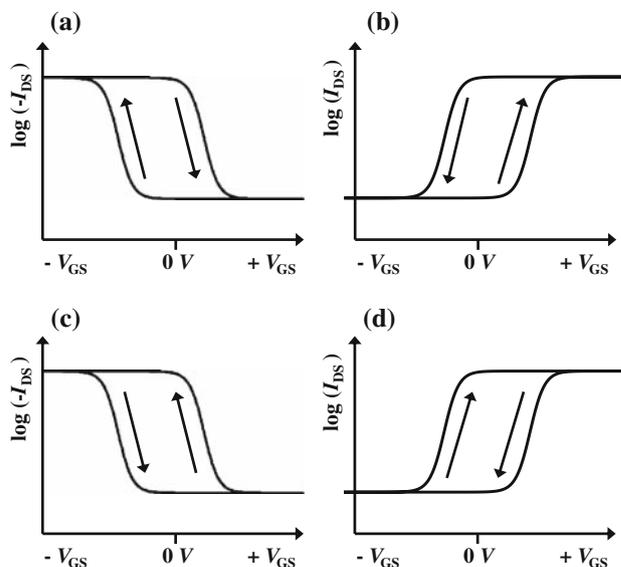


Fig. 2 Schematic transfer characteristics (I_{DS} vs. V_{GS}) of p-type (a, c) and n-type (b, d) OFETs. a and b show higher BSC hysteresis. For p-type OFETs (a), this higher BSC hysteresis turns clockwise, whereas for n-type OFETs (b), this hysteresis turns counterclockwise. c and d show lower BSC hysteresis

sweep current. For p-type OFETs, the direction of this hysteresis is clockwise, whereas for n-type OFETs the turning direction is anticlockwise. Figure 2c and d show schematic transfer characteristics where the back sweep current is lower than the forward sweep current. To avoid ambiguities, the notation “higher back sweep current hysteresis” (or “higher BSC hysteresis”) and “lower BSC hysteresis” is used in this paper. Lower BSC hysteresis is very often attributed to charge carrier trapping close to the channel, whereas higher BSC hysteresis is usually caused by mobile ions in the dielectric, or by (ferroelectric) polarization of the dielectric.

Threshold voltage shifts are frequently reported in the literature due to bias stress [45–47]. Bias stress is the application of a (usually) constant V_{GS} for an extended time. This bias stress causes instabilities that may lead to either hysteresis, if the bias stress effect occurs to a large extent reversibly with V_{GS} , or to degradation, if the bias stress effect is irreversible with V_{GS} . Hysteresis and degradation may have the same physical origin [48]. The direction of the shift is such that a fully turned on OFET slowly turns itself off and vice versa [47, 49]. Recovery is sometimes possible; this follows a power law in terms of time dependence and may take a few days in the dark [47]. Investigations of the threshold voltage shift under illumination suggest that traps at the interface may be responsible for the observed shift [49–51].

Bias stress in an OFET can also cause a change in effective field effect mobility, which is attributed to an irreversible structural change in the semiconductor due to the electrostrictive effect [52]. The change is independent of the trapping and detrapping of mobile charge carriers caused by bias stress. Such electric field-induced mechanical strains are also discussed as failure modes in inorganic high-electron-mobility transistors [53].

Measuring hysteresis

A collection of IEEE Standard Test Methods for the characterization of organic transistors and materials has been published [54]. According to this standard, it is recommended that the forward and reverse sweeps should be measured to ensure that no hysteresis is present and thus prevent incorrect calculations of OFET parameters. However, there is currently no generally accepted procedure for measuring hysteresis in OFETs.

The hysteresis can be characterized by the transfer characteristics of OFETs or by the capacitance–voltage [C(V)] characteristics of corresponding metal–insulator–semiconductor (MIS) structures. C(V) characteristics are used to distinguish between p- and n-type semiconductors: the depletion layer acts as a capacitance in series to the dielectric, changing the total capacitance, so a high

capacitance is measured in the accumulation regime. In this paper, hysteresis effects mainly based on evaluating the transfer characteristics of OFETs are discussed.

As shown above, the hysteresis can be interpreted as a shift of the threshold voltage depending on the gate voltage sweep direction. Therefore, a simple definition of V_{th} in an OFET with hysteresis cannot be given. Both the V_{th} in the off-to-on sweep and the V_{th} in the on-to-off sweep as well as the size of the hysteresis often depend on the sweep rate, the start and end voltage of the sweep, the step width, the delay time, the hold time and the step delay time [55]. A comparison of different devices is therefore difficult or impossible if these parameters are not defined.

Hysteresis due to reversible effects can only be seen in the transfer characteristics when the sign of V_{GS} is changed during the measurement, preferentially with a symmetric sweep around $V_{GS} = 0$ V (e.g., sweep $-V_{GS}$ to $+V_{GS}$ and back). Without changing the sign of V_{GS} , the measurement may only reveal degradation due to bias stress effects.

Reversible hysteresis effects such as those described in this article cannot be measured with output characteristics (I_{DS} vs. V_{DS}) [56]. During such a measurement, V_{GS} is changed in steps from V_{th} (ideally 0 V) to the on state (e.g., $+V_{GS}$ for n-type OFETs). The sign of the applied V_{GS} usually does not change during an output measurement. If differences between the forward and the backward scan are observed in the output characteristics, this usually reflects a continuous increase or decrease in I_{DS} due to bias stress.

The pulsed measurement method [50, 51, 57, 58] is a way to measure hysteresis-free characteristics of OFETs, even when the OFET normally shows hysteresis. The idea of the gate pulse method is to apply off voltage (depletion voltage) to the device being tested after each measurement point. The measurement voltage (V_x) is applied for a certain short time. At the end of the pulse, I_{DS} is measured, and then the off voltage is applied for a longer period. During this long off pulse, the changes due to the measurement pulse [polarization, (de)trapping, ...] are usually reversed. This procedure is repeated for each step. OFET characteristics measured with this pulse method do not show hysteresis if the pulse lengths are chosen properly. However, such OFETs may show hysteretic characteristics in a normal sweep measurement of the transfer characteristics. Though the pulsed method may be used to obtain device parameters like mobilities, it should be accompanied by conventional symmetric sweeps with different sweep rates to rule out memory effects.

Quantifying hysteresis

Several quantifications for the magnitude of the hysteresis have been suggested: half width at mid-capacitance [59], maximum gate voltage shift at a given I_{DS} [60], or average

I_{DS} for a given V_{GS} [61]. Quantifying the hysteresis as a shift in V_{th} for a given sweep rate may also provide a way to compare different devices. Hysteresis phenomena are based on dynamic processes that depend heavily on the time of the measurement and on the duration of the applied voltage. These parameters can change the size of the hysteresis and also the slopes of the curves. Therefore, strict rules (e.g., a refined IEEE standard [54]) may be useful to ensure a comparable quantification.

Hysteresis mechanisms

Many physical effects that cause hysteresis in OFETs are mentioned in the literature. Some of these effects are identical to those already explained for inorganic transistors. Given the complex nature of hysteresis in OFETs, the underlying effects, as shown in Fig. 1, can be grouped according to the location within the device where the effect acts [62]:

- (A) *Effects close to or in the semiconductor channel (near the semiconductor/dielectric interface):* (A1) trapped majority or minority charges in the channel close to the semiconductor/dielectric interface, (A2) charge injection from the semiconductor into the dielectric, (A3) slow reactions (e.g., bipolaron formation) of mobile charge carriers and (A4) mobile ions in the semiconductor
- (B) *Bulk effects of the dielectric:* (B1) polarization of the dielectric (ferroelectric or “quasi-ferroelectric” polarization) and (B2) mobile ions in the dielectric
- (C) *Charge injection from the gate into the dielectric*

(A1) Trapped majority or minority charges in the channel close to the semiconductor/dielectric interface

Traps at the semiconductor/dielectric interface can result in lower BSC hysteresis. There are various traps in organic layers such as impurities, structural defects (e.g., the effective conjugation length of a polymer can slightly change its HOMO–LUMO levels) and self-trapping (the charge polarizes its surroundings, which again stabilizes the position of the charge) [49, 63, 64]. If the rate of release of charge from such a trap is sufficiently low, the sweep rate may be faster than the time necessary to reach thermal equilibrium, which results in hysteresis effects in the electric characteristics of the device [64].

Various material combinations show lower BSC hysteresis due to traps [60]; examples are pentacene transistors on thermally grown SiO_2 [65] as well as on sol–gel cast SiO_2 [66], pentacene on various organic dielectrics [67] or C_{60} on a triple layer of SiO_2 /zirconium-silicon oxide/ SiO_2 [68]. Oxygen or water can influence this trap-caused hysteresis

[38, 69–73], and oxygen or water can also change the bias stress effect [74–78]. OH groups are presumed to act as electron traps [79–81]. Self-assembled monolayers (SAMs) [68, 79, 82, 83] and dielectrics without OH groups [84] are known to reduce these traps and change the mobility [85–87]. In ambipolar OFETs, hysteresis due to charge carrier trapping is frequently observed [57, 88–92].

Dielectrics with low k values (low- k dielectrics) increase the mobility and reduce the hysteresis [16, 93–95]. High- k dielectrics covered with a thin flat layer of a low- k dielectric result in OFETs with low voltage and high mobility [96, 97], whereas a rough interface causes additional traps, resulting in increased hysteresis [98, 99].

Both types of charge carriers (holes and electrons) can be trapped. For a p-type semiconductor, holes are the majority carriers and electrons are the minority carriers. Trapping majority or minority carriers results in lower BSC hysteresis, as schematically shown in Fig. 3.

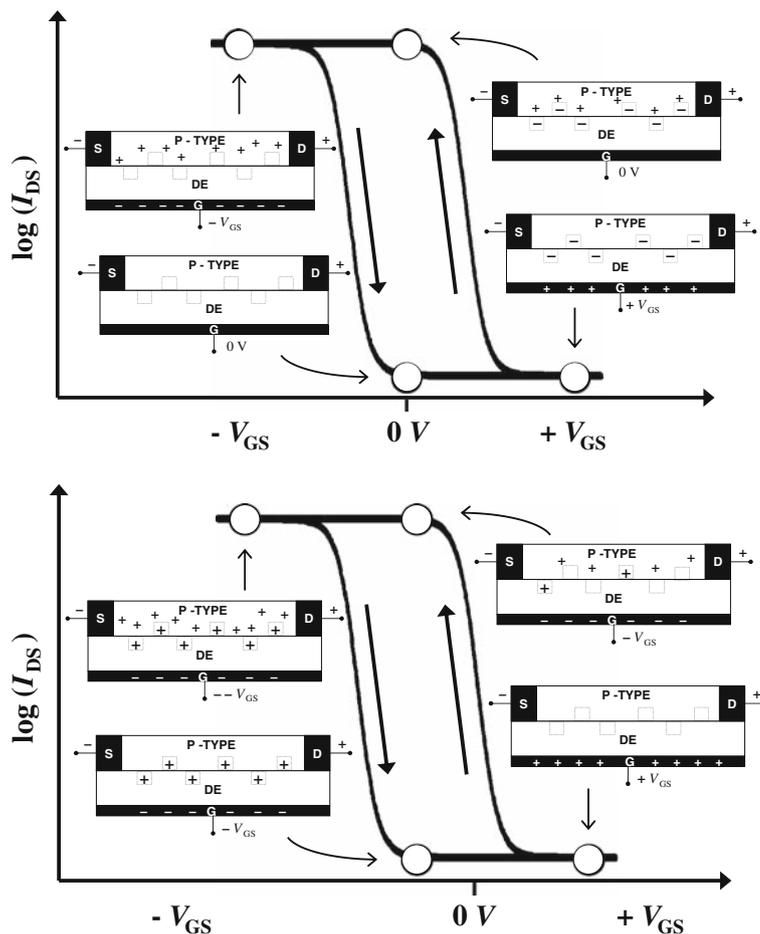
Modeling and second harmonic generation measurements show that hole and electron traps must be assumed [100, 101].

Minority traps

Long-lifetime minority traps (e.g., electron traps in pentacene) that fill fast and empty slowly can cause hysteresis, as shown in Fig. 3. Long-lifetime deep electron traps are suggested for pentacene on SiO_2 [37, 73, 102]. At the start of the sweep in the on state (negative V_{GS} for pentacene), all electron traps are empty. Upon applying an off voltage (positive V_{GS}), the traps are quickly filled. When sweeping rapidly from off to on, the negatively charged traps induce more (mobile) positive charges than correspond to the given V_{GS} field. These excess holes cause higher I_{DS} in the forward sweep. In the on state, all traps are emptied, causing lower I_{DS} in the back sweep. The faster the forward sweep, the greater the number of filled traps and the higher I_{DS} . This explains why the size of this hysteresis increases for fast sweeps.

Gu et al. [102] discuss whether negative or positive charges are trapped in pentacene/octadecyltrichlorosilane/ SiO_2 OFETs. They conclude that stored negative charges, most likely electrons, in pentacene dominate the observed shift in V_{th} . The first hint that this is the case was obtained by comparing the different sweep directions in the transfer characteristics for high negative V_{GS} : when sweeping in the off-to-on direction, the electron traps are slowly emptied, causing V_{GS} -dependent mobility and nonlinear transfer characteristics. During the on-to-off sweep, the electron traps are already empty. This does not change for negative V_{GS} , and therefore I_{DS} versus V_{GS} is linear. To confirm this mechanism, time domain measurements were performed. First, a predefined starting voltage V_{GS0} was applied. After quickly changing to $V_{GS} = -20$ V, the change in I_{DS} with

Fig. 3 Lower BSC hysteresis for p-type OFETs caused by trapping of minority charge carriers (top) or trapping of majority charge carriers (bottom). The circles indicate the location of the respective cartoon. Open square, empty trap; plus symbol in a square, trapped hole; minus symbol in a square, trapped electron; plus symbol in a circle, cation; minus symbol in a circle, anion; plus symbol, hole; minus symbol, electron; S, source; D, drain; G, gate; DE, dielectric; thick arrow, dipole orientation



time (at fixed $V_{GS} = -20$ V and $V_{DS} = -10$ V) was monitored. Depending on the applied voltages V_{GS0} (before the measurement), I_{DS} was either constant or decreased with time, as shown in Fig. 4.

If electron acceptor states dominate the observed effect, these states are initially filled when a positive gate voltage V_{GS0} is applied. The trapped electron population slowly decays by detrapping after V_{GS} is switched from the positive V_{GS0} to -20 V. I_{DS} decays in a similar manner, since the decaying trapped electron population results in a decaying extra hole population that balances it. Accordingly, when a more negative V_{GS0} (e.g., -50 V) is used initially, all traps are emptied. After switching to -20 V, all of the traps are still empty, and no change in I_{DS} over time due to slow detrapping is expected. If hole traps cause the observed hysteresis, the opposite behavior will be expected [37, 73, 102]. Scanning Kelvin probe microscopy can also show which type of charge carrier is trapped at the channel [103].

Majority traps

Majority traps (e.g., hole traps in pentacene) that fill fast and empty slowly can also result in lower BSC hysteresis,

as shown in Fig. 3. When the scan is started from the off state, the traps are empty. During the off-to-on sweep, the traps get filled. In the case of pentacene OFETs, for example, each negative value of V_{GS} corresponds to a certain number of field-induced holes. Some of the holes are quickly trapped. During the on-to-off sweep, the trapped holes are slowly released (much slower than the sweep rate), and so fewer mobile holes are in the channel at any given V_{GS} and the resulting I_{DS} is lower [37, 102]. The release rate of the traps must be slower than the scan rate, meaning that fast sweeps show larger hysteresis than slow sweeps. This dependence on the scan rate is important for distinguishing between different hysteresis mechanisms.

Ucurum et al. performed similar measurements on pentacene/SiO₂ OFETs. They concluded that trapped holes (majority charge carriers) cause the hysteresis. They also developed an equivalent circuit PSpice model that is able to simulate the observed hysteresis and the observed time dependence assuming trapped holes [104, 105].

Yoon et al. [60] investigated four n-type and two p-type semiconductors, each on four different substrates. Figure 5 shows the transfer characteristics for 24 investigated OFETs. Various trapping-type hysteresis effects are observed.

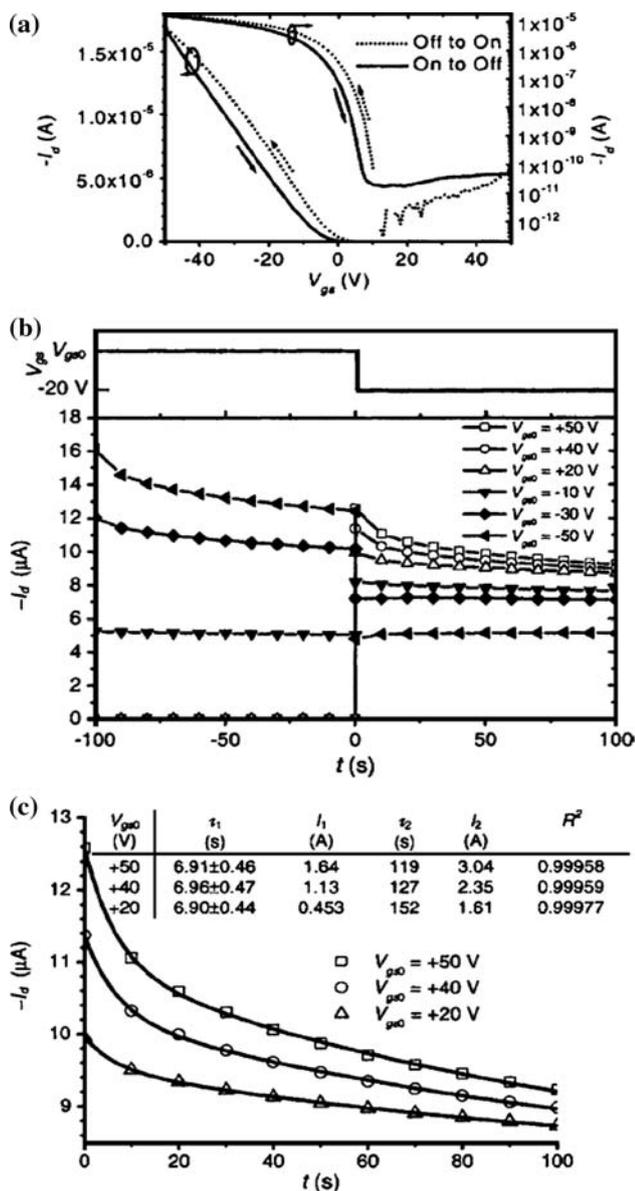


Fig. 4 **a** Transfer characteristics of a pentacene/octadecyltrichlorosilane/SiO₂ OFET, $V_{DS} = -10$ V, for sweeps in both directions. **b** Time domain measurement data for the same device. The *upper panel* depicts the applied V_{GS} waveform, and the *lower panel* shows the measured $-I_{DS}$ data. **c** Fitting results. *Symbols* are measured data and *solid lines* are fits. Reprinted with permission from [102]; copyright 2005, American Institute of Physics

However, they could not be directly correlated to a certain dielectric or to a certain semiconductor. Trap-caused hysteresis in OFETs is determined by the semiconductor/dielectric material combination and not by just one material (semiconductor or dielectric) alone.

Goldmann et al. [56] showed that bias stress effects and hysteresis are closely related. Deep and shallow traps at the interface of the dielectric with the semiconductor are emptied over different timescales: shallow traps are

emptied quickly, causing hysteresis, whereas deep traps that are emptied over a much longer time scale (e.g., hours) cause a shift in V_{th} known as the bias stress effect. Figure 6 shows both effects: hysteresis and bias stress of a SiO₂/rubrene single-crystal OFET. Stressing with negative gate voltages fills all of the hole traps, resulting in a smaller hysteresis after the bias stress, whereas positive gate voltage stress empties all of the traps, resulting in an increased hysteresis after the stress [55, 56].

(A2) Charge injection from the semiconductor into the dielectric

This mechanism is very similar to the charge-trapping mechanism. The only difference is the location of the “traps.” Charge is injected from the semiconductor into the dielectric. From a device point of view, this injected charge can also be seen as traps that cause lower BSC hysteresis [106–109]. Katz et al. [110] proposed electrets that show reversible hysteresis due to charge injection as a form of memory. Baeg et al. put a chargeable electret [e.g., poly(α -methylstyrene) (P α MS)] between the SiO₂ dielectric and the pentacene in order to build a memory device. A critical voltage is needed to switch the device. Characterizing the OFET with voltages below this critical switching voltage results in hysteresis-free characteristics [111, 112].

Charge injection from the semiconductor into the dielectric resembles floating gate memory transistors, where an additional metal layer (the floating gate) is inserted into the dielectric [113]. Floating gate transistors are well known in inorganic technology [41]. The injected charges are quasi-permanently stored in the floating metal layer and influence the gate field. This additional polarization contributing to the gate field can be seen as a change in the threshold voltage of the transistor. Floating gate OFETs have a certain threshold voltage that is required in order to inject charges into the floating gate. An ideal floating gate shows no hysteresis upon measuring the transfer characteristics below this threshold, whereas cyclic sweeps above this threshold show hysteresis. Floating gate OFETs [106] and all-organic floating gate OFETs [114] were recently demonstrated [113].

(A3) Slow reactions of mobile charge carriers

In general, lower BSC hysteresis is attributed to the trapping of charge carriers (A1), but there are examples that contradict the trapping mechanism: reducing the sweep rate (slower measurements) causes an increase in the hysteresis, pointing to species with low mobility. Measuring at increased temperature increases the hysteresis and also

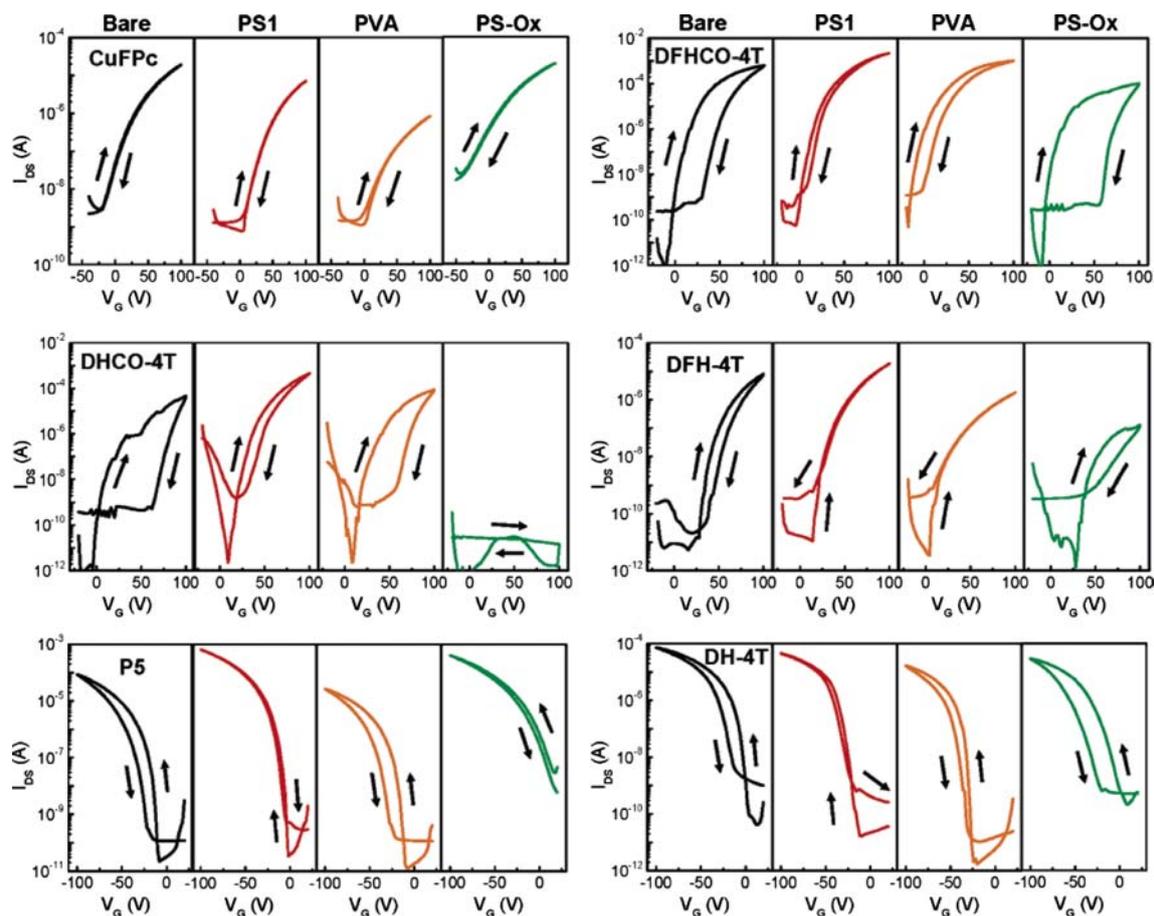


Fig. 5 Comparison of forward and backward transfer characteristics of OFETs fabricated with the indicated organic semiconductor/dielectric combinations (see [60] for details). *Arrows* denote the gate

bias sweep direction. Reprinted with permission from [60]; copyright 2006, American Chemical Society

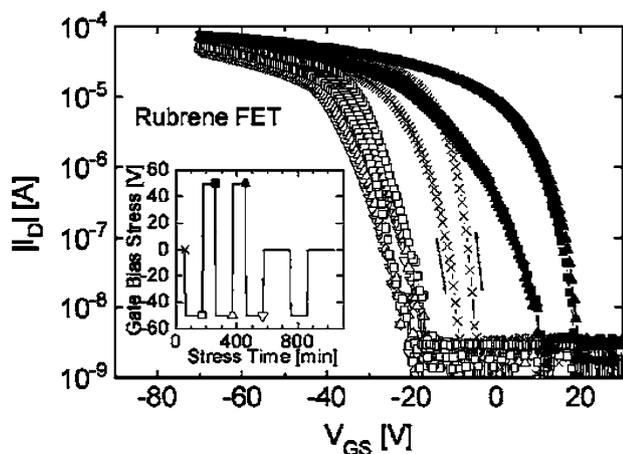


Fig. 6 Evolution of the transfer characteristics of a rubrene/SiO₂ single-crystal FET ($V_{DS} = -10$ V) during a bias stress sequence: I - V characteristics before stress (*cross symbols*) and at the end of the different periods of negative (*open symbols*) and positive (*filled symbols*) bias stress are shown. The *inset* shows the measurement protocol for the applied stress as well as the positions in time of the different I - V measurements. Reprinted with permission from [56]; copyright 2006, American Institute of Physics

shifts the curves. Ions (e.g., iodine) influence this hysteresis, but the complexity suggests that a second mechanism is present in the device [115, 116]. Simulations show that traps cannot explain the observed hysteresis [117]. As the subthreshold slope is closely related to interface traps [100, 118, 119], hysteresis in OFETs with a high subthreshold slope cannot be explained by traps [120].

A polaronic/bipolaronic mechanism has been suggested in order to explain this lower BSC hysteresis observed in OFETs with conjugated polymers [121–123]. In the on state of an OFET, a high charge carrier density is induced in the semiconductor close to the dielectric interface. Charge carriers in conjugated polymers can be described as polarons or bipolarons. It is suggested that, due to the very high polaron density, some polarons overcome the coulomb repulsion and form doubly charged bipolarons. If mobile counterions (e.g., charged impurities) are present, these might stabilize the polaron or bipolaron due to the neutralization of their charge. The different properties of polarons and bipolarons, their slow rate of formation and their complexation with counterions may cause the lower BSC hysteresis [121, 123–126].

Theoretical predictions have been presented and verified experimentally [122, 127].

It should be mentioned that there is still an ongoing discussion in the literature as to whether bipolarons exist in organic semiconductors or not. All of the theoretical considerations can also be explained by the formation of polaron–polaron complexes other than bipolarons, such as dimerization [128]. This dimerization would lead to σ bonds that should be detectable.

(A4) Mobile ions in the semiconductor

Ions in the semiconductor can also cause lower BSC hysteresis. This effect is the opposite to that caused by mobile ions in the dielectric. Mobile ions in the semiconductor that have the same polarity as majority carriers move slowly to the channel. As the total number of charges at the channel is fixed (determined by the applied voltages and the device parameters), ions reduce the number of mobile charges at the channel. This mechanism also decreases the I_{DS} , causing lower BSC hysteresis [129]. As ions move slowly, this hysteresis is expected to be larger for slower sweep rates, which provides the opportunity to distinguish between traps and mobile ions. In principle, ions in the semiconductor that have charge of the opposite sign to the majority charge carriers could also cause lower BSC hysteresis (majority and minority traps both cause lower BSC hysteresis), but there do not appear to be any examples of this in the literature.

Li ions diffuse in and out of the depletion layer of a poly(3-hexylthiophene (P3HT)/Al Schottky contact, causing a stable hysteresis in the I – V characteristics of the diode. The polymer layer is mixed with ethylene carbonate, a plasticizer that is known [130, 131] to increase the mobility of inorganic ions [132]. Mobile Na^+ ions diffuse under the influence of an applied voltage from a substrate into an organic semiconductor above the substrate, where

the ions cause hysteresis in the I – V characteristics [133]. Nanotube-based OFETs coated with a layer containing Na^+ ions show lower BSC hysteresis, because the ions can diffuse to the channel and thereby decrease the “on” current. The authors observed that humidity increases the hysteresis, while evacuating the device drastically decreases the hysteresis [129].

(B1) Polarization of the dielectric (ferroelectric or “quasi-ferroelectric”)

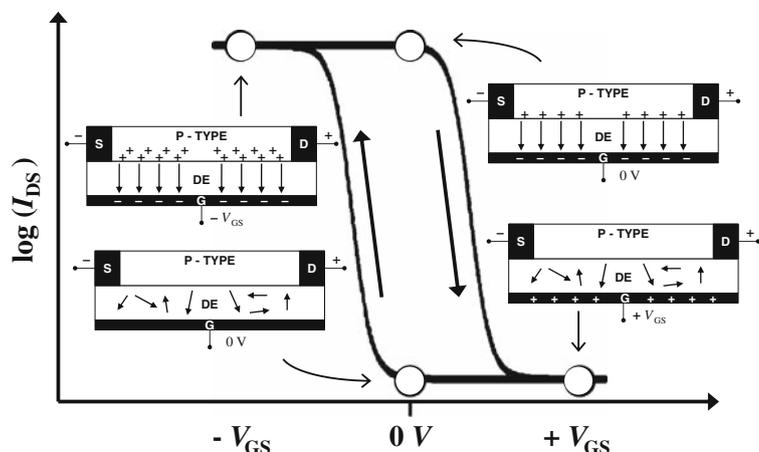
Ferroelectrics as dielectrics

Ferroelectric dielectrics are materials that show remanent polarization due to an externally applied electric field. This remanent polarization causes an electric field in addition to the gate field, and so ferroelectric dielectrics cause higher BSC hysteresis, as shown in Fig. 7.

A coercive voltage must be applied to reduce the polarization (the charge displacement) to zero. This transition voltage scales with the thickness of the ferroelectric: the thicker the layer, the higher the coercive voltage [134]. The hysteresis loop saturates when the whole material is polarized [135].

In general, a ferroelectric material placed between two electrodes [metal–insulator–metal (MIM) structure] can be polarized in both directions, depending only on the applied field. The strong electric field of the remanent polarization is stabilized by neutralizing charges in the metal electrodes, which reduce the depolarizing field [28, 29, 136]. The situation can be different in a metal–insulator–semiconductor (MIS) structure; in general, only one type of charge carrier is mobile in an organic semiconductor, and so the ferroelectric can be polarized in only one direction, as shown in Fig. 7. The higher BSC hysteresis resulting from the use of ferroelectric gate dielectrics appears to be a promising approach to memory elements, but problems

Fig. 7 Higher BSC hysteresis for p-type OFETs caused by (ferroelectric) polarization. For a guide to the symbols, see the caption of Fig. 3



with the long-term stability of the induced polarization, a known problem with inorganic ferroelectrics, have not yet been addressed.

The first ferroelectric OFET (FerrOFET) using an inorganic ferroelectric was demonstrated in 2001 [137]. Other materials [138] and the first all-organic FerrOFET followed [139, 140]. The material used by Schroeder is not strictly ferroelectric, but ferroelectric-like with molecular dipoles that are quasi-permanently oriented in an external electric field. Such devices have since improved [141], and a solution-processed FerrOFET using poly(vinylidene fluoride/trifluoroethylene) (P(VDF/TrFE)) as organic ferroelectric insulator and poly[2-methoxy,5-(2'-ethylhexyloxy)-*p*-phenylene-vinylene] (MEH-PPV) as organic semiconductor has been demonstrated [142]. The annealing temperature of P(VDF/TrFE) is 140 °C, which makes it compatible with processing on organic substrates. The on-off ratio after a week (i.e., programming once and reading the data for a week) was still 10^4 . The programming time required to achieve an on-off ratio of 10^3 was 0.5 ms [142]. Similar results were obtained for p-type and n-type FerrOFETs using P(VDF/TrFE) as ferroelectric insulator and MEH-PPV and PCBM as semiconductors, respectively [143]. Figure 8 shows the transfer curves; higher BSC behavior can be seen in both cases.

Further improved devices [134, 144, 145], ambipolar FerrOFETs [146] and FerrOFET arrays [147] have been demonstrated, but products using FerrOFETs as memory elements are not yet available on the market [113].

“Quasi-ferroelectric” polarization of the dielectric

When the dielectric contains polar groups (e.g., polar side groups, short polymer chains, residual solvent) that can slowly move or reorient due to an external electric field, these dielectrics cause an effect that is very similar to ferroelectric materials, and so it is often called “quasi-

ferroelectric” (in ferroelectric materials the polarization is a thermodynamically stable state). Slow metastable polarization of the dielectric also causes higher BSC hysteresis [37, 110], as shown in Fig. 7.

Poly(vinyl phenol) (PVP) is known to cause hysteresis due to polarization in the dielectric, resulting in higher BSC hysteresis [148]. As this effect is due to mobile dipoles in the bulk, the size of the hysteresis scales with the thickness of the PVP layer [62]. Furthermore, the size of the hysteresis heavily depends on the sweep rate, with larger hysteresis seen for slower sweep rates [149]. In addition, the water content, especially when working under ambient conditions, influences the hysteresis [59]. The size of the hysteresis can be decreased or even removed by thermally crosslinking the PVP [62, 65, 149, 150]. However, different crosslinking procedures may have different effects on the hysteresis: extending the crosslinking time or reducing the amount of volatile species by vacuum treatment reduces the hysteresis, whereas UV exposure causes an increase in hysteresis [149].

Materials other than PVP, even those without polarizing dipoles, can be electrostatically charged during device fabrication in order to influence the properties of the device. If the charging is not changed during device operation, the OFET shows no hysteresis; on the other hand, if standard device operation changes the charging of the dielectric, hysteresis may be observed [151].

(B2) Mobile ions in the dielectric

Mobile ions in the dielectric also cause higher BSC hysteresis. The effect on the device is very similar to that seen for polarization of the dielectric (Fig. 7), as can be seen from Fig. 9, which schematically shows the higher BSC hysteresis resulting from mobile ions in the dielectric for an n-type OFET.

Fig. 8 Hysteretic drain current as a function of gate voltage of FerrOFETs. **a** n-type FerrOFET with PCBM as semiconductor and a 1.7 μm thick ferroelectric P(VDF/TrFE) insulator layer at a drain voltage of 10 V. **b** p-type FerrOFET with MEH-PPV on P(VDF/TrFE) that was previously put into the off state. Reproduced with permission from [143]; copyright 2005, Wiley-VCH Verlag GmbH & Co. KGaA

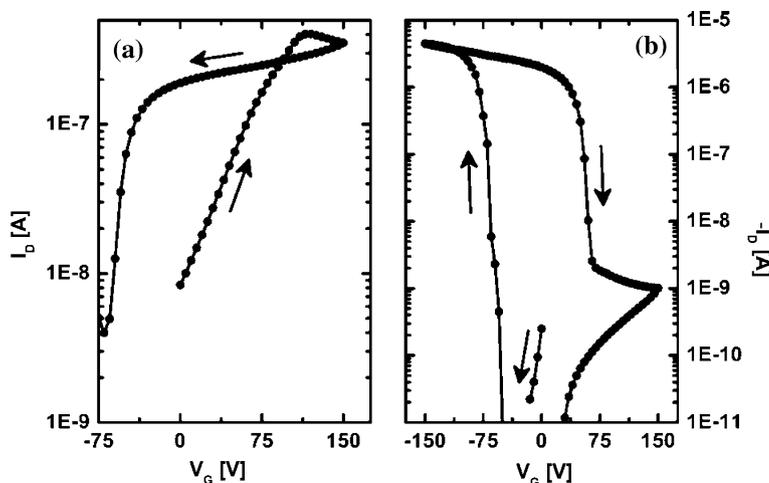
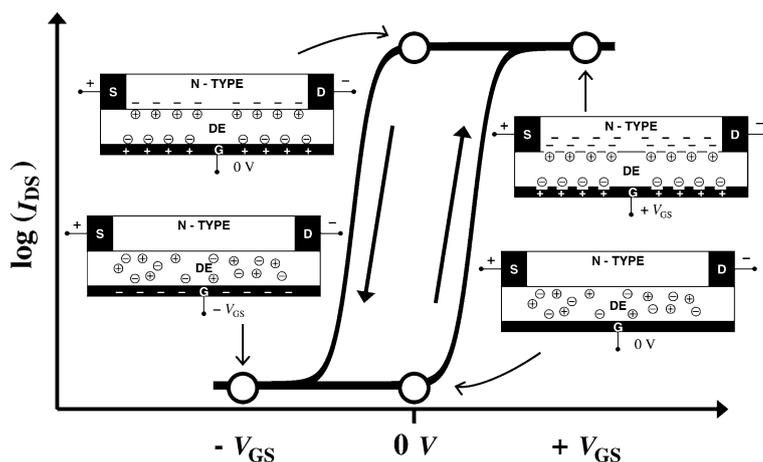


Fig. 9 Higher BSC hysteresis for n-type OFETs caused by mobile ions in the dielectric. For a guide to the symbols, see the caption of Fig. 3



Upon applying an “on” voltage (in this case a positive V_{GS}) to the gate, the cations move towards the semiconductor. When V_{GS} is swept back to 0 V (backward sweep), the ions stay close to the semiconductor, thereby retaining the diminishing field and causing higher BSC hysteresis [152]. More ions accumulate close to the semiconductor when the on voltage is applied for longer, and so hysteretic phenomena increase with decreasing sweep rate. Consequently, faster sweep rates result in smaller hysteresis. The sweep rate dependence of the hysteresis is different to the dependence seen when charge carriers at the gate/dielectric interface are trapped (mechanism C), which may help to distinguish between these two mechanisms.

As already pointed out, ions are known to cause threshold voltage shifts in inorganic transistors [22–24]. In general, ions are at least as mobile in organic materials as in SiO_2 , so it is expected that they should cause even more pronounced effects in organic materials. Ions in PMMA [153], in cyanoethylpullulan [16, 154] and in deoxyribonucleic acid (DNA) [155, 156] are proposed to cause the observed hysteresis. Na^+ ions diffusing from soda lime glass into the dielectric cause higher BSC hysteresis [149]. Water influences the ionic hysteresis in devices using poly(vinylcinnamate)/poly(vinylidene-fluoride/tetrafluoroethylene/hexafluoropropylene) double layers [97] or PVP [157] as dielectrics.

Polyelectrolytes are typical dielectrics with mobile ions. They are expected to reduce the operating voltage of OFETs due to their strong polarizability, but these OFETs show higher BSC hysteresis [158]. Detailed investigations of OFETs with poly(vinyl alcohol) (PVA) as dielectric and methanofullerene-[6,6]-phenyl-C61-butyric acid-methyl ester (PCBM) [159, 160] or MDMO-PPV [91] as semiconductors showed pronounced hysteresis in the transfer characteristics. The hysteresis decreased with decreasing temperature, indicating that mobile ions are the reason for this hysteresis [161]. The situation is even more complex when ambipolar charge transport processes are investigated.

Hysteresis effects from mobile ions have been observed in addition to ambipolar charge transport [162].

Egginger et al. studied the effect of mobile ions in PVA in more detail [152]. During PVA synthesis, sodium acetate is a byproduct that is not completely removed from the PVA polymer during the cleaning steps after synthesis. Rigorous cleaning by dialysis resulted in quasi-hysteresis-free Buckminsterfullerene C_{60} /PVA OFET characteristics, as shown in Fig. 10.

Figure 10 shows an OFET built with the as-received PVA (a) and an OFET with the cleaned PVA (b). Intentionally adding small amounts of sodium acetate to the PVA solution before casting the film resulted in a strong increase in the hysteresis [152]. Figure 11c and d show hysteresis, indicating that traces of ions are present even in the cleaned PVA. The hysteresis appears when measuring the transfer characteristics at elevated temperature (the mobility of ions is exponentially dependent on temperature). The change in ion mobility is reversible: cooling to room temperature results in hysteresis-free behavior. A similar effect is observed (Fig. 11a, b) when an OFET with the as-received PVA is cooled; cooling “freezes” the ions and thereby drastically decreases the hysteresis. The presence of ions and ion movement in PVA has been verified with dielectric spectroscopy [152]. Increases in both the permittivity and the loss angle at frequencies below the loss maximum due to electrode polarization [163, 164] or Maxwell–Wagner polarization [165–167] appear at sufficiently high temperatures. Both effects are attributed to ionic conductivity with a broad distribution of relaxation frequencies [152, 168, 169].

For most applications, mobile ions should be avoided in organic integrated circuits in order to minimize device instability. However, immobilized ions at the semiconductor/metal interface can improve charge injection [170]. Electroluminescence and the photovoltaic effect have been demonstrated at ionic junctions [171], and nanoionic resistive switching for memory applications was recently reviewed [172].

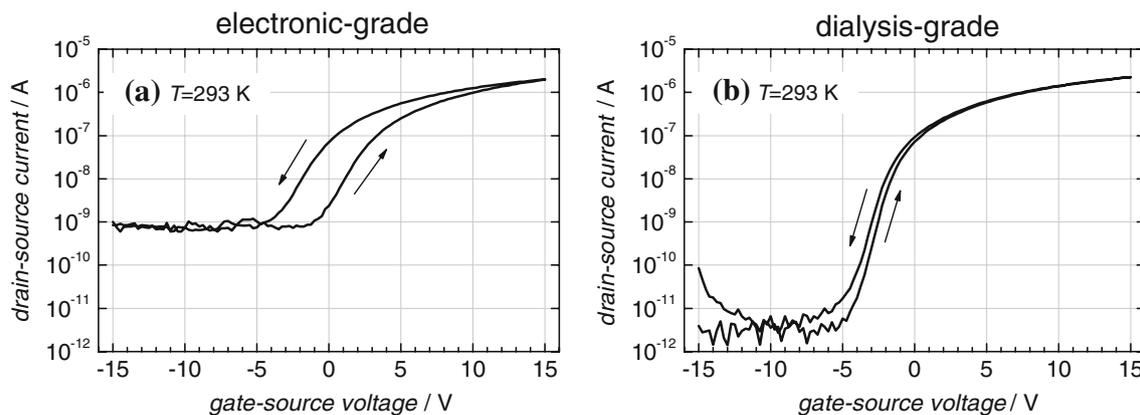


Fig. 10a–b Transfer characteristics of C_{60} field-effect transistors with two different grades of PVA gate dielectrics at room temperature (sweep rate 70 mV/s). The transistor with the uncleaned (“electronic-grade”) dielectric shows a clear hysteresis (a). The transistor with the

cleaned (“dialysis-grade”) dielectric shows almost no hysteresis (b). Reproduced with permission from [152]; copyright 2008, Wiley-VCH Verlag GmbH & Co. KGaA

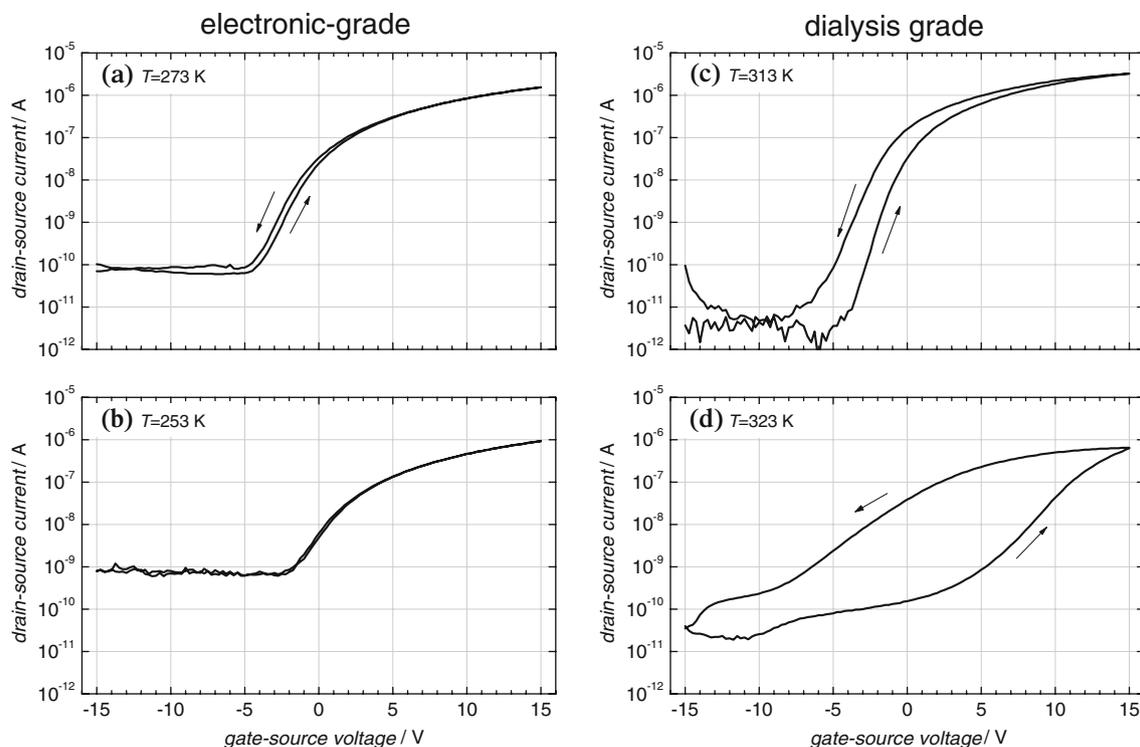


Fig. 11a–d Transfer characteristics of the OFETs characterized in Fig. 10, measured at different temperatures (sweep rate 70 mV/s). The hysteresis of the transistor with the electronic-grade dielectric is significantly reduced at 273 K (a) and almost disappears at 253 K (b).

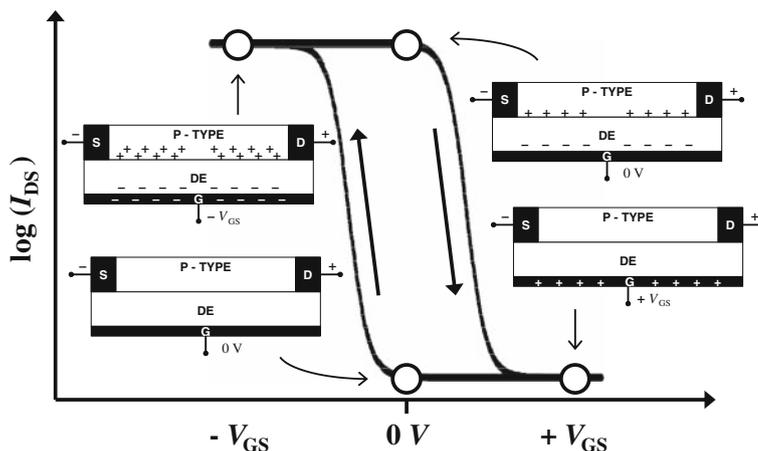
The transfer characteristics of the transistor with the dialysis-grade dielectric open up and show a distinct hysteresis at 313 K (c), which becomes very broad at 323 K (d). Reproduced with permission from [152]; copyright 2008, Wiley-VCH Verlag GmbH & Co. KGaA

(C) Charge injection from the gate

If charges can be injected from the gate electrode into the dielectric, these charges also cause higher BSC hysteresis. This mechanism is shown in Fig. 12 for a p-type semiconductor and for electrons injected from the gate into the dielectric.

In the on state (negative V_{GS}), electrons are injected from the gate into the dielectric. Upon reducing V_{GS} to 0 V, the electrons stay in the dielectric, thereby stabilizing the accumulated holes forming the channel. In most cases, the electrons remain for only a short time, and so fast sweep rates cause large hysteresis whereas slower sweep rates decrease the higher BSC hysteresis [173]. The size of the

Fig. 12 Charge injection from the gate into the dielectric causing higher BSC hysteresis in OFETs. For a guide to the symbols, see the caption of Fig. 3



hysteresis also strongly depends on the maximum gate voltage. Inserting a blocking layer between the gate electrode and the dielectric reduces the observed hysteresis [62, 157, 173–175].

Usually, floating gate transistors use charge injection from the semiconductor into the dielectric [41, 113]—compare with mechanism (A2)—but in some transistor systems it is also possible to inject charges from the gate to the floating gate [176, 177].

Combined mechanisms

Using TiSiO as gate insulator, electrons can be injected from the semiconductor into the dielectric, causing lower BSC hysteresis, or electrons can be injected from the gate into the dielectric, causing higher BSC hysteresis [178]. In addition, the solvent used to cast the semiconductor can drastically influence the size of the hysteresis [179]. The strongest effect determines the direction and the size of the hysteresis if more than one hysteresis mechanism is present [62]. It has been suggested that one hysteresis could be neutralized by making use of an additional effect causing another hysteresis in the other direction. Experimentally, the total hysteresis was reduced by balancing the effects [180]. However, problems with the long-term operational stability of the device will most probably occur.

Summary

A variety of effects (charge trapping at the semiconductor/dielectric interface, charge injection from the semiconductor into the dielectric, slow reaction of mobile charge carriers, mobile ions in the semiconductor, polarization of the dielectric, mobile ions in the dielectric, or charge injection from the gate into the dielectric) that cause hysteresis in OFETs are summarized in this paper. More than

one of these mechanisms are often present in the same device.

As hysteresis strongly depends on the measured parameters, it is necessary to know the applied voltages and the measurement details to be able to compare different results. To separate hysteresis from bias stress effects, hysteresis must be measured in cyclic sweeps with V_{GS} symmetric around 0 V.

On the one hand, hysteresis in transistors and other device elements must be avoided when designing integrated circuits; on the other hand there are potential applications of reversible hysteresis in nonvolatile memory devices [113]. However, stringent requirements [181] must be met for memory devices based on hysteresis effects, and so far none of the proposed organic systems have succeeded in meeting these requirements. Therefore, in the field of organic electronics, it is crucial to fully understand, characterize and control hysteresis phenomena in OFETs.

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