

High mobility, low voltage operating C₆₀ based n-type organic field effect transistors

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ABSTRACT

We report on C₆₀ based organic field effect transistors (OFETs) that are well optimized for low voltage operation. By replacing commonly used dielectric layers by thin parylene films or by utilizing different organic materials like divinyltetramethyldisiloxane-bis(benzocyclo-butene) (BCB), low density polyethylene (PE) or adenine in combination with aluminum oxide (AlOx) to form a bilayer gate dielectric, it was possible to significantly increase the capacitance per unit area (up to two orders of magnitude). The assembly of metal-oxide and organic passivation layer combines the properties of the high dielectric constant of the metal oxide and the good organic–organic interface between semiconductor and insulator provided by a thin capping layer on top of the AlOx film. This results in OFETs that operate with voltages lower than 500 mV, while exhibiting field effect mobilities exceeding 3 cm² V⁻¹ s⁻¹.

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1. Introduction

Since the first reports on organic field effect transistors (OFETs) in the late 1980s [1], tremendous progress in OFET technology has been made [2–4]. Recent investigations have been focused mainly on the improvement of charge carrier mobility with the result that organic devices are now displaying field effect mobility values of more than 1 cm² V⁻¹ s⁻¹ and are therefore competing with amorphous silicon based devices. A major obstacle on the way to reach large scale industrial application is the lifetime and stability of the fabricated devices. With this respect, significant progress has been made in the past years as well. On the one hand successful reports of encapsulation to protect the sensitive organic layer from oxygen and water vapor have emerged [5–8]. On the other hand attempts have been made in order to find materials that exhibit increased intrinsic stability under ambient conditions [9]. Another key issue is represented by the operational voltage of OFETs, which is of critical importance in many thinkable applications, like radio frequency identification tags or light emitting devices [10–12]. As a matter of fact it is necessary to reduce the applied voltages to values in the order of 1 V or lower for any mobile application.

To understand the possibilities to reduce the operating voltages, it is necessary to take a look on the theoretical background of OFETs. The conventional equation that describes the dependence of the source-drain current of an OFET on the applied voltages (Eq. (1)) shows, that in order to reduce the gate- and source-drain-voltages at a given current value there are three possible paths. Either the geometry factor W/L , the capacitance per unit area C_0 , or the mobility μ have to be increased accordingly. The first quantity cannot be altered to a large extent because the channel length L is limited by the manufacturing procedures, e.g. shadow mask deposition or printing, to about 10 μm . Furthermore, a reduction of channel length leads to a domination of the contact resistance over the channel resistance, which inhibits saturation of the channel current [13,14]. A significant increase of the channel width W on the other hand leads to a bigger area necessary for one device, which represents a drawback for integrated circuits. The second quantity μ is a material property and cannot be increased to a large extent.

$$I_D = \frac{W}{L} \cdot \mu \cdot C_0 \cdot \left(V_G - V_T - \frac{V_D}{2} \right) \cdot V_D \quad (1)$$

There are however two ways to improve the capacitance per unit area. Firstly, to reduce the thickness of the dielectric layer and secondly, to use materials with a higher dielectric constant. In the last 10 years a lot of work was published on the topic of high-k materi-

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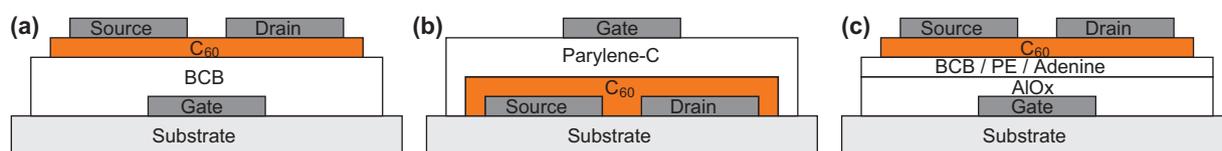


Fig. 1. Device geometries: (a) BCB- C_{60} , (b) C_{60} -parylene, and (c) AlOx-organic- C_{60} .

als applied in low voltage OFETs as reviewed by Ortiz et al. [15]. The first attempts using insulators with higher dielectric constant were reported in 1999 achieving operational voltages in the 5 V regime in pentacene based OFETs [16,17]. OFETs utilizing high- k dielectrics often suffer from problems like charge trapping at the active interface, high gate leakage or that successive growth of high quality layers of organic semiconductors is hindered by high surface roughness [18,19]. Consequently layered structures consisting of high- k and standard low- k organic dielectrics were used to combine the advantages of both material types.

In this work we pursue the goal to reduce the operational voltage to values below 1 V. The necessary increase in the geometric capacitance C_0 is addressed by reducing the thickness of the dielectric layer and by using high- k materials. As a starting point we decided to use state of the art C_{60} based OFETs with BCB gate dielectric, because they were reported to exhibit good performance parameters like mobility values up to $6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [20]. In this case, the increase of capacitance per unit area can be achieved by reducing the layer thickness, with the drawback that the leakage current rises significantly. Parylene-C on the other hand allows fabrication of electrically dense films with a thickness reduced by approximately a factor of 10 as compared to BCB. Since the dielectric constant of parylene-C is only 3 [21], the utilization of a material with higher dielectric constant like a metal oxide became necessary. AlOx exhibits a dielectric constant of 9 and is therefore very well suited for this purpose [22], with the only drawback that the interface between AlOx and C_{60} is less favorable as compared to BCB- C_{60} [23]. Consequently we decided to employ thin organic capping layers on top of AlOx in order to combine the advantages of both high dielectric constants and organic-organic interfaces.

2. Experimental

The preparation procedure of bottom gate BCB- C_{60} OFETs is described in detail elsewhere [20]; the device geometry is shown in Fig. 1(a) and the layer thicknesses and the aspect ratio W/L of the devices are presented in Table 1.

In case of the device utilizing parylene-C as a gate dielectric, we used a top gate structure as depicted in Fig. 1(b). Clean glass was used as a substrate and 60 nm thick Al source and drain contacts were deposited through a shadow mask by thermal evaporation at a pressure of 10^{-6} mbar. The gate length was $L = 80 \mu\text{m}$ and the channel width was $W = 2 \text{ mm}$, which resulted in a W/L ratio of 25. Next,

300 nm of C_{60} was deposited via hot wall epitaxy (HWE) [24] at a substrate temperature of 150°C and a base pressure of 10^{-6} mbar, followed by parylene deposition carried out in a homemade reactor via a three-zone process. First the dimer di-chloro-di-p-xylylene is evaporated at a temperature of 100°C , next the vapor is passing a high temperature zone (700°C) where pyrolysis leads to cleavage of the dimers. The resulting monomers are finally deposited at room temperature on the sample surface, where they spontaneously polymerize to form a transparent and conformal thin film. The process is carried out at a pressure of 10^{-2} mbar and for the OFET fabrication a dielectric layer thickness of 225 nm was used. The last step was represented by the deposition of a 60 nm thick Al gate contact through a shadow mask.

The third type of fabricated devices were standard bottom gate devices, with an inorganic/organic double layer structure gate dielectric, as sketched in Fig. 1(c). In each case AlOx was used as the bottom layer, followed by capping with an organic layer. AlOx was prepared by anodization of a 200 nm layer of vacuum deposited Al in 0.01 mol citric acid, as explained in detail by Stadler et al. and references therein [23]. The anodization voltage was $V_A = 40 \text{ V}$ that led to a film with a thickness of $\sim 52 \text{ nm}$. In the case of AlOx-BCB devices, the BCB precursor used in forming stand alone BCB dielectric films was diluted in mesitylene to produce $\sim 10 \text{ nm}$ thick spin coated films on AlOx. In the case of adenine, the films were formed by thermal evaporation in an Edwards evaporator at a pressure of $\sim 10^{-6}$ mbar. The film thicknesses and deposition rates were 10 nm and 1 nm s^{-1} respectively. Low density polyethylene (Aldrich) was evaporated up to a thickness of 2 nm at a rate of 0.01 nm s^{-1} . Information concerning evaporation of polymers, especially PE is given elsewhere [25–27]. On top of these structures a 300 nm thick C_{60} layer and 100 nm Al source and drain electrodes were deposited as in the case of devices built on a dielectric layer consisting of BCB only.

All measurements were carried out at room temperature under N_2 atmosphere inside a glove box, to avoid exposure to ambient humidity and oxygen. The transistor characteristics were recorded with an Agilent E5273A 2-channel-source unit.

3. Results and discussion

First we present the starting point of this work, which is a C_{60} OFET with a $2 \mu\text{m}$ BCB dielectric having a capacitance per unit area of 1.2 nF cm^{-2} . In Fig. 2(a) the transfer characteristics of this device

Table 1

Properties of investigated devices and materials; $|V_{max}|$ is the absolute maximum applied gate- or source-drain-voltage in the corresponding transfer characteristic. d_1 is the thickness of the first dielectric layer and d_2 is the thickness of the second dielectric layer in the case of bilayer structures (the same is valid for the dielectric constants $\epsilon_1 + \epsilon_2$). Ad stands for adenine. Dielectric constants for AlOx and adenine are taken from [22], for BCB from [31] and for parylene from [21].

	BCB	Parylene	AlOx-BCB	AlOx-Ad	AlOx-PE
$ V_{max} $ (V)	60	4.5	0.4	0.8	0.75
μ ($\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)	5.1	4.6×10^{-2}	3.5	3.2	2.9
V_T (V)	13.2	-3.5	-3×10^{-3}	-0.25	0.39
on/off	$>10^6$	$\sim 10^{2.5}$	$\sim 10^{2.5}$	$\sim 10^3$	$>10^3$
C_0 (nF cm^{-2})	1.2	11.8	92.7	106	133
ϵ_1/ϵ_2	2.65	3	9/2.65	9/3.85	9/2.3
d_1/d_2 (nm)	2000	225	52/10	52/10	52/2
W (mm)	3	2	3	2	2
L (μm)	35	80	50	80	80

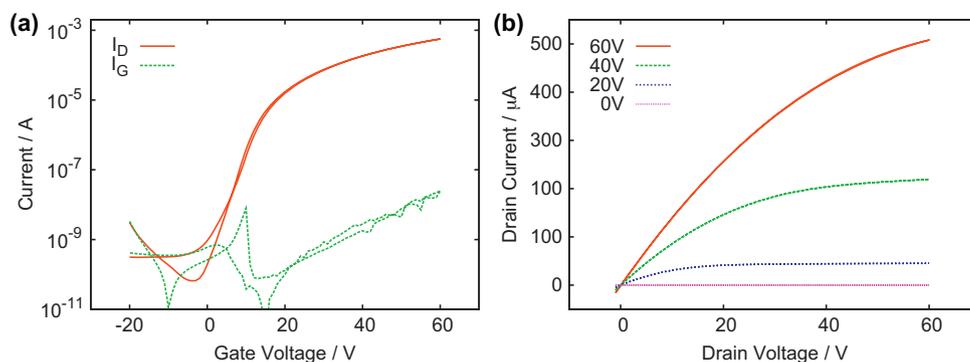


Fig. 2. (a) Transfer characteristics of a device using BCB as a dielectric measured at $V_D = 60$ V. (b) Corresponding output curves at gate voltages from $V_G = 0$ V to $V_G = 60$ V.

are presented showing a high on-off ratio of the device ($>10^6$). The red curve shows the OFET characteristics in saturation regime (at $V_D = 60$ V) exhibiting a maximum drain current of $I_D = 0.56$ mA whereas the green curve shows the leakage current of the device, which is always below $I_G = 25$ nA. The charge carrier mobility calculated from the transfer curve is $5.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [28]. The inverse subthreshold slope is 3.1 V/decade and the threshold voltage is relatively high ($V_T = 13.2$ V). Output characteristics of this device are shown in Fig. 2(b) at different gate voltages.

To reduce the operational voltages, we replaced BCB with parylene-C, which allowed us to prepare electrically dense films at a significantly reduced layer thickness. These devices were prepared in a top gate structure, since we found that the parylene layer degrades when used in a bottom gate device, leading to high leakage currents. The reason for this is presumably the heat treatment of the parylene film under high vacuum conditions during the subsequent deposition of C_{60} . Top-gate configuration of OFETs offers an additional advantage over bottom-gate OFETs, in that the devices are protected from environmental degradation by encapsulation due to the passivation layer deposited on top and hence become more stable. The crucial point in the preparation of top-gate OFETs is the surface roughness of the semiconducting layer, which gives the active interface where the charge transport takes place. Due to this restraint, it is not possible to use C_{60} of high crystallinity (usually prepared with HWE at a substrate temperature of 250°C [20]), because in this case the surface roughness would be too high. An optimal trade-off between a flat surface and big crystallites was found to be a growth temperature of 150°C for C_{60} . Another point that is of major importance is the thickness of the parylene layer. In principle parylene should give conformal pinhole-free layers down to about 10 nm [29]. However we found that a layer thickness of 225 nm was necessary to generate reliably working devices with a

low leakage current, a fact that could be connected to the C_{60} surface roughness as well. The capacitance of the dielectric layer was approximately a factor of 10 higher (11.8 nF cm^{-2}) as compared to the device having BCB as gate dielectric, therefore the required gate voltage could be reduced significantly. After an optimization of the thickness of the parylene film and the surface morphology of C_{60} film, we finally achieved a low operating voltage device (4.5 V), with a leakage current lower than 0.1 nA. Fig. 3(a) and (b) shows the characteristics of C_{60} -parylene OFET in top-gate configuration. These OFETs have an on-off ratio of $\sim 10^{2.5}$, a mobility of $4.6 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a threshold voltage of -3.4 V, giving devices working in depletion mode. The reduced mobility and the threshold voltage shift as compared to the BCB devices is surprising, keeping in mind that high performance OFETs employing parylene as a dielectric were fabricated by other groups [6,30]. In the case presented in this work, this behaviour could be related to the fact that the C_{60} surface is exposed to air during transport from the HWE to the parylene deposition chamber. Thus contaminants like O_2 and H_2O were possibly trapped at the active interface between organic semiconductor and the dielectric layer.

Further reduction of the operating voltage is presented in Fig. 4. In this case the operating voltage is reduced to values below 1 V by changing the dielectric layer from a single layer to a bilayer of AlOx and a thin organic capping film. The metal oxide with a thickness of 52 nm leads to increased capacitance and the organic passivation layer gives the benefits of the organic-organic interface to improve the performance of the OFETs. The total capacitance of these devices is in the range of 90 – 130 nF cm^{-2} . Notably, the hysteresis is also very low for all employed capping layers on AlOx . Fig. 4(a) shows the transfer characteristics of the $\text{AlOx}/\text{BCB}/\text{C}_{60}$ OFETs working at very low voltages (0.4 V) exhibiting a relatively high mobility of $3.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a very low threshold voltage of approximately

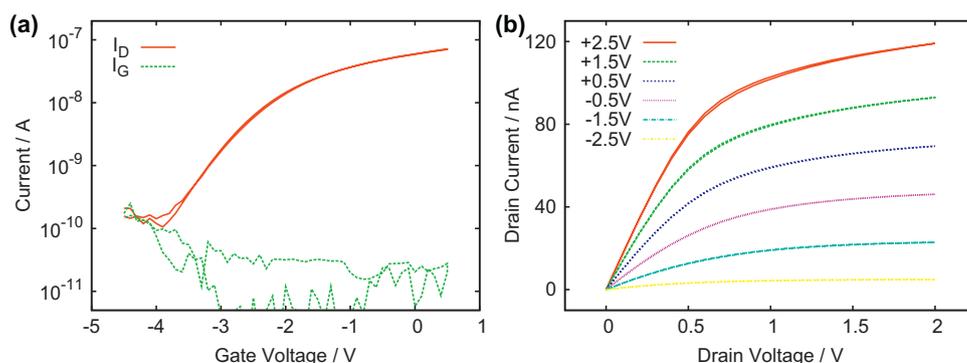


Fig. 3. (a) Transfer characteristics of a device using parylene-C as a gate insulator measured at $V_D = 2$ V. (b) Corresponding output curves at gate voltages from $V_G = -2.5$ V to $V_G = +2.5$ V.

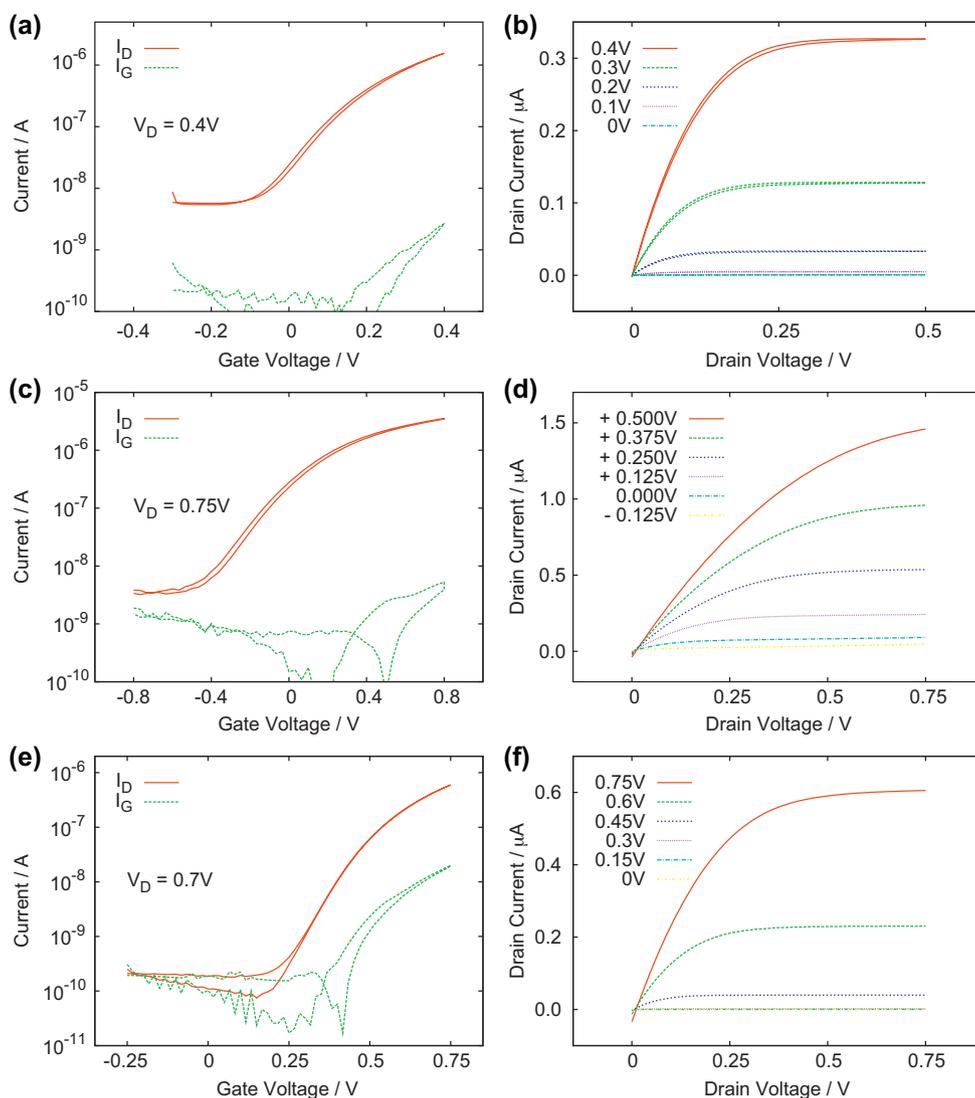


Fig. 4. Transfer and output characteristics of: (a) and (b) AIOx-BCB OFET; (c) and (d) AIOx-adenine OFET; (e) and (f) AIOx-PE OFET.

-3×10^{-3} V. In part (b) the output characteristics are shown for gate voltages ranging from 0 V to 0.4 V. Fig. 4(c) and (d) shows the transfer and output characteristics of the OFETs fabricated using thin adenine layers as passivation films for AIOx. The field effect mobility and threshold voltage values are $3.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and -0.25 V respectively. Similarly in Fig. 4(e) and (f) data of OFETs fabricated on very thin evaporated polyethylene films for interface engineering on the AIOx dielectric layer is presented. The field effect mobility is $2.9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and the threshold voltage is $V_T = 0.39$ V. The collected results and different device parameters are summarized in Table 1.

4. Conclusion

We have shown that it is possible to significantly reduce the operational voltage for C_{60} OFETs by reducing the dielectric layer thickness and by utilizing materials with high dielectric constants like metal oxides. The best performing device presented in this study exhibits a high mobility and is working with a very low threshold voltage ($\mu = 3.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $V_T = -3 \times 10^{-3}$ V), which was achieved by replacing a $2 \mu\text{m}$ BCB dielectric layer by a bilayer structure consisting of 52 nm AIOx and 10 nm BCB. Thereby the operating voltage is reduced from 60 V to 0.4 V , permitting fab-

rication of integrated circuits powered by commercially available batteries.

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