

Electrical response of highly ordered organic thin film metal-insulator-semiconductor devices

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We report a detailed investigation of the electrical properties of organic field-effect transistors (OFETs) and metal-insulator-semiconductor (MIS) capacitors formed from highly ordered thin films of C₆₀ as the active semiconductor and divinyltetramethyl disiloxane-bis(benzocyclobutene) (BCB) as the gate dielectric. Current-voltage measurements show the OFETs to be n-channel devices characterized by a high electron mobility (~ 6 cm²/V s). An equivalent circuit model is developed which describes well both the frequency and voltage dependences of the small-signal admittance data obtained from the corresponding MIS capacitors. By fitting the circuit response to experimental data, we deduce that increasing gate voltages increases the injection of extrinsic charge carriers (electrons) into the C₆₀. Simultaneously, the insulation resistance of the BCB decreases, presumably by electron injection into the insulator. Furthermore, the admittance spectra suggest that the capacitance-voltage (*C-V*) behavior originates from a parasitic, lateral conduction effect occurring at the perimeter of the capacitor, rather than from the formation of a conventional depletion region.

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I. INTRODUCTION

Thin-film organic field-effect transistors (OFETs) based on the symmetric C₆₀ molecule have shown high charge carrier mobility in the range 3–6 cm²/V s, thus establishing a benchmark for n-type organic semiconductors.^{1–7} The electrical response of OFETs is generally probed by modulating the conductance at the semiconductor-insulator interface with a gate voltage, V_G , applied normally to the interface. In particular, the dependences of source-drain current I_D , on V_G , temperature, and source-drain gap L are used to establish the nature of charge injection and transport mechanism in such devices. However, large variations in the experimental data on even nominally the same sample^{8,9} make it difficult to draw unambiguous conclusions as to processes occurring in the device.

Small-signal measurements on metal-insulator-semiconductor (MIS) capacitors and directly on OFETs^{10–18} provide an alternative method for investigating such processes. A combination of admittance spectra and capacitance-voltage (*C-V*) data provides a wealth of information not only on the semiconductor layer, e.g., doping density and bulk mobility,¹¹ but also on the interface between semiconductor and gate dielectric,^{10,11,19} e.g., the density of states for interface traps.²⁰ Admittance spectroscopy and *C-V*

measurements on p-type pentacene¹⁸ and poly(3-hexylthiophene)^{16,21} based MIS capacitors and OFETs have been reported already. However, no reports have yet appeared of similar measurements on MIS capacitors fabricated from high mobility electron transporting materials such as thin crystalline films of C₆₀.

In this paper, we present both the output and transfer characteristics of OFETs formed from highly crystalline thin films of C₆₀ grown on divinyltetramethyl disiloxane-bis(benzocyclobutene) (BCB) together with the admittance spectra of MIS capacitors employing the same materials. The results show that the threshold voltage is related to the injection of extrinsic charge carriers into the semiconductor and that “depletion” arises from reduced injection rather than from the formation of a space-charge layer of ionized dopants that is typical of conventional silicon devices.

II. EXPERIMENTAL

OFETs and MIS diodes were fabricated using patterned indium tin oxide (ITO)-coated glass slides as the gate electrode/substrate. The slides were cleaned using acetone, 2-propanol, Helmanex glass cleaning solution, and finally with de-ionized H₂O in an ultrasonic bath. The gate dielectric, BCB^{2–4} purchased from Dow Chemicals, was dissolved in mesitylene and spin coated onto the ITO substrate and cured at 250 °C for 2 h in a vacuum oven. C₆₀ cleaned by sublimation was used as received from MER Corp. After curing the BCB, a 300 nm thick film of C₆₀ was grown by hot wall epitaxy at a temperature $T_s = 250$ °C and with a base vacuum of 10^{–6} mbar. A shadow mask was used to pattern

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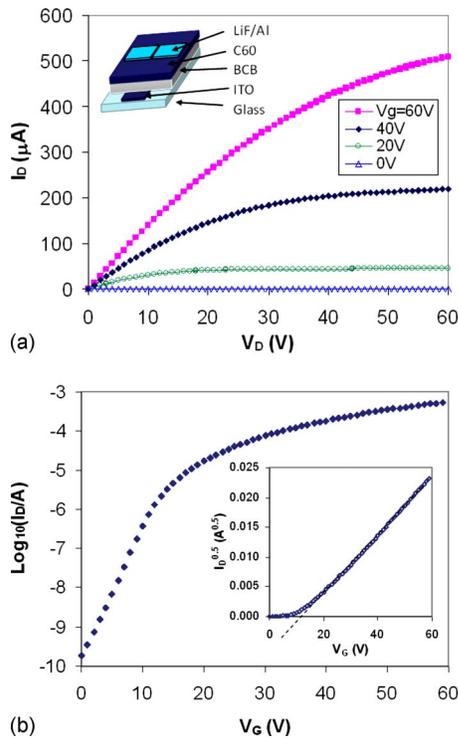


FIG. 1. (Color online) (a) Output characteristics of the C_{60} OFET. The device structure is shown in the inset. (b) The transfer characteristics of the same device obtained at $V_D=60$ V, plotted as $\log I_D$ vs V_G (main diagram) and as $I_D^{0.5}$ vs V_G in the inset.

the C_{60} film which was of the same high crystalline quality as that reported previously.² Devices were completed by evaporating top-contact electrodes consisting of LiF/Al (0.6 and 60 nm thick, respectively) under high vacuum ($\sim 10^{-6}$ mbar) using a shadow mask placed in the same holder as before to ensure optimum registration with the gate electrode under the C_{60} film. The structure of the devices is shown in the insets of Figs. 1 and 3. The channel length (L) and width (W) in the OFET were 30 μm and 1.5 mm, respectively. The MIS capacitors were prepared in such a way that all the layers had an active area of $3 \times 3 \text{ mm}^2$. The average thickness of the dielectric was typically in the range 1–1.5 μm . Device transportation from the hot-wall reactor to the glove box for top-contact evaporation was carried out under ambient conditions.

Electrical characterization of the OFETs was carried out in an Oxford Instrument DNV Optistat with a base pressure of 10^{-6} mbar. An Agilent parametric measurement system (model E5273A with two source-measure units) was employed for the steady-state current-voltage measurements. All measurements were performed at a scan rate of 2 V/s.

The small-signal response of the MIS capacitors was measured over a wide frequency range using an HP 4248A precision LCR meter and applying to the gate electrode a probe signal of 0.1 V superimposed on a bias voltage, V_G . Capacitance-voltage (C - V) measurements were made at 1.2 kHz by incrementing/decrementing V_G through the range ± 40 V at a rate of 0.02 V/s. Admittance spectra were obtained over a wide range of frequencies at several predetermined values of V_G . The thicknesses of the dielectric and

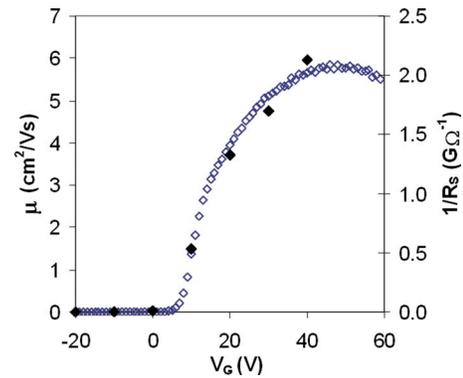


FIG. 2. (Color online) Gate voltage dependence of the mobility (open diamonds) calculated from the local slope of the OFET transfer characteristic in Fig. 1(b). Also shown (closed diamonds) is the reciprocal of the sheet resistance of the semiconductor contributing to the lateral conduction effects at the perimeter of the MIS capacitor.

organic layers were measured under ambient conditions with a Digital Instrument Dimension 3100 atomic force microscope.

III. RESULTS AND DISCUSSION

A. dc characteristics of the OFETs

Figure 1 shows (a) the output and (b) the transfer characteristics of the C_{60} OFETs. These are well described by the conventional equations for the dependence of drain current I_D on gate voltage V_G and drain voltage V_D , i.e.,

$$I_D = \frac{W}{L} \mu C_i \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right] \quad (1)$$

and

$$I_D = \frac{W}{L} \mu C_i \frac{(V_G - V_T)^2}{2} \quad (2)$$

in the linear and saturation regimes, respectively. Here, W/L (~ 50) is the aspect ratio of the OFET, μ is the effective mobility in the channel, and C_i ($\sim 1.4 \pm 0.2 \text{ nF/cm}^2$) is the capacitance per unit area of the gate dielectric. From the plot of $\sqrt{I_D}$ versus V_G , [inset of Fig. 1(b)], the threshold voltage V_T is deduced to be ~ 11 V.

Transport in the accumulation channel of OFETs is generally assumed to occur by hopping through localized states so that μ depends on V_G , through control of state occupancy. The form of the gate-voltage dependence may be deduced from the *local* slope of the $\sqrt{I_D}$ versus V_G plot,²² i.e.,

$$\mu = \frac{W}{2LC_i} \left(\frac{d\sqrt{I_D}}{dV_G} \right)^2 \quad (3)$$

and is plotted in Fig. 2. As can be seen, μ increases rapidly through the subthreshold region ($V_G < 11$ V) attaining a maximum value of $\sim 5.8 \text{ cm}^2/\text{V s}$ when $V_G \sim 45$ V but then decreases slowly above ~ 50 V. Departure from this maximum value may be expected, since Eq. (3) ceases to be valid as device operation moves from the saturation to the linear regime at higher V_G . Contact resistance effects may also be a factor in such behavior.²³

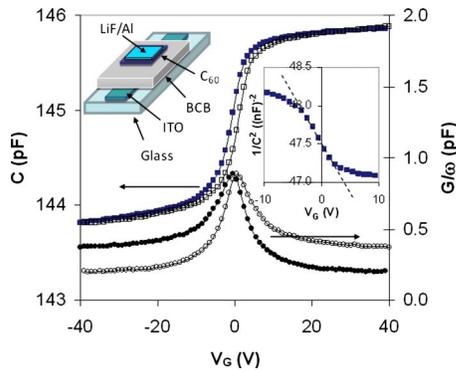


FIG. 3. (Color online) Capacitance (C) and loss (G/ω) measured at 1.2 kHz when sweeping the gate voltage V_G from -40 V (closed symbols) and then from $+40$ V (open symbols). The inset (top left) depicts the structure of the MIS capacitor. When plotted in Mott–Schottky format (Ref. 24), the capacitance data show good linear behavior over part of the range (right inset).

B. Voltage dependence of capacitance and conductance

In Fig. 3 the capacitance C and loss G/ω (conductance/angular frequency) of the C_{60} MIS capacitors measured at 1.2 kHz are plotted as functions of V_G . The sharp decrease in capacitance as V_G sweeps from positive to negative bias is consistent with the formation of a depletion region in the C_{60} film. Furthermore, the peak occurring in the G/ω versus V_G plot for depletion voltages is consistent with the presence of interface states.²⁰ Replotting the capacitance data in the Mott–Schottky format,²⁴

$$\frac{1}{C^2} = \frac{1}{C_I^2} + \frac{2}{\varepsilon\varepsilon_0qN_D A^2}(V_G - V_{FB}), \quad (4)$$

where ε is the relative permittivity of the C_{60} film, ε_0 is the permittivity of free space, C_I is the capacitance of the insulator, q is the electronic charge, N_D is the donor doping density, A is the device area, and V_{FB} is the flat band voltage, yields a linear region for V_G in the range ± 5 V (see inset of Fig. 3) from which a donor doping density, $N_D \sim 2 \times 10^{16} \text{ cm}^{-3}$, is deduced. Although this is a reasonable value, we show in Sec. III C that the step change in capacitance in Fig. 3 does not arise from the creation of a space-charge layer of ionized donors in the semiconductor.

C. Frequency dependence of capacitance and loss

The frequency dependence of capacitance and loss of the MIS diode are plotted in Fig. 4 for a range of V_G . Two dispersions are clearly visible:

- (i) a high frequency process whose central frequency shifts from ~ 50 to ~ 100 kHz for increasing accumulation voltages and
- (ii) a process which occurs at low frequency for depletion voltages but shifts to higher frequencies, eventually merging with the high frequency process, as V_G increases in the accumulation regime.

The rapid rise in loss at the highest frequencies suggests also the presence of a third dispersion arising from a series

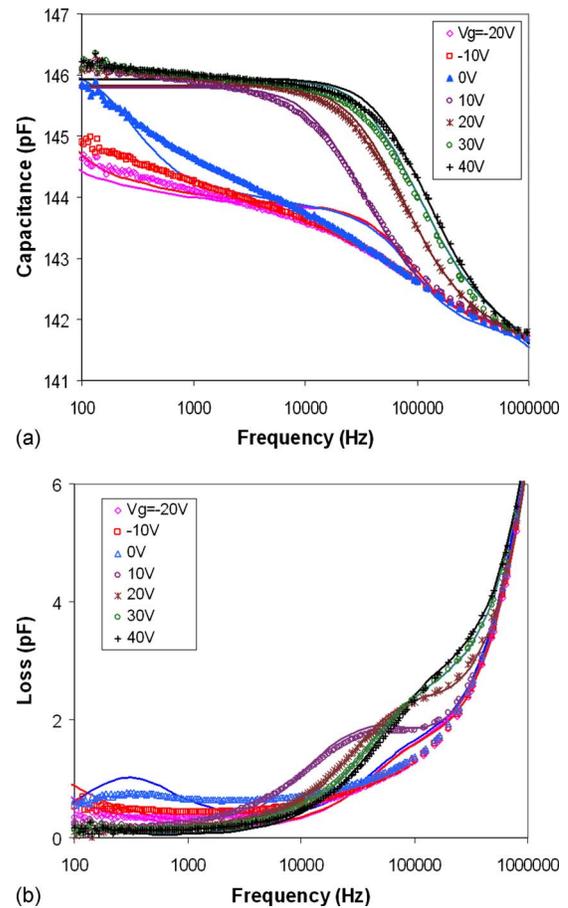


FIG. 4. (Color online) Frequency dependence of (a) capacitance C and (b) loss G/ω measured for various voltages applied to the ITO electrode. The solid curves are numerically generated fits based on Eqs. (5)–(9) and the parameters in Table I.

resistance, R_C , associated with the electrodes.¹¹ In the following, we concentrate on the origin of the two main dispersions.

An ideal MIS capacitor is composed of two dielectric layers [Fig. 5(a)] and may be represented by the section of the equivalent circuit labeled “Diode” in Fig. 5(b). Here, R_B and C_B represent the resistance and capacitance of the bulk C_{60} layer, R_I and C_I , and the resistance and capacitance of the insulator, all defined by the area of the LiF/Al electrode [Fig. 5(a)]. R_C is a series resistance associated with the con-

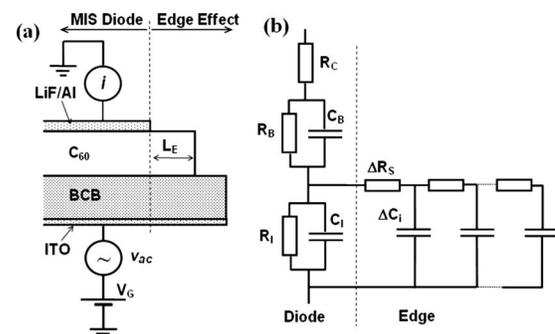


FIG. 5. (a) Partial cross section of the MIS capacitor showing the origin of the edge effect. (b) The equivalent circuit of the diode showing the contributions from the main capacitor structure and from the presence of excess semiconductor of width L_E at the electrode perimeter.

TABLE I. Parameter values used to obtain the theoretical plots in Fig. 4.

V_G (V)	-20	-10	0	10	20	30	40
C_I (pF)	143.8	143.8	143.7	143.5	143.4	143.5	143.5
R_I (Ω)	1×10^{13}	1×10^{13}	1×10^{13}	8×10^9	8×10^9	8×10^9	8×10^9
C_B (nF)	11.0	11.0	11.0	12.0	11.5	11.0	10.5
R_B (Ω)	160	160	160	220	113	80	75
R_C (Ω)	52	50	53	50	47	49	48
C_E (pF)	2.44	2.44	2.44	2.30	2.44	2.44	2.44
$R_S L_E^2 / A_E$ (Ω)	5×10^9	3×10^9	5.5×10^8	8×10^6	3.2×10^6	2.5×10^6	2×10^6

tacts. It is known from recent studies of parasitic effects in MIS capacitors²⁵⁻²⁷ that lateral conduction at the electrode edge can make significant contributions to the low frequency capacitance of MIS capacitors with unpatterned bottom electrodes. In the present work, an attempt was made to eliminate this effect by creating a ‘‘mesa’’ structure in which the top contact was aligned with the patterned semiconductor layer. However, we believe that sufficient semiconductor was left uncovered to give rise to an edge effect in which carriers drifting through the protruding semiconductor of length L_E [Fig. 5(a)] charge the insulator capacitance lying under the excess semiconductor. The effect of such lateral conduction is represented by the distributed RC network in Fig. 5(b), where R_S is the sheet resistance (Ω/sq) of the semiconductor layer and C_i is the capacitance per unit area of the insulator.

The total admittance, Y , presented by the circuit in Fig. 5(b) is given by

$$Y = G + j\omega C = (Y_I^{-1} + Y_B^{-1} + R_C)^{-1}, \quad (5)$$

where $j = \sqrt{-1}$, G and C are the measured conductance and capacitance of the device (assumed to be in parallel), and where

$$Y_B = (R_B^{-1} + j\omega C_B) \quad (6)$$

and

$$Y_I = (R_I^{-1} + j\omega C_I) + (G_e + j\omega C_e). \quad (7)$$

C_e and G_e represent the edge effect and are given by²⁶

$$C_e = \frac{C_E}{\alpha} \cdot \frac{\sinh \alpha + \sin \alpha}{\cosh \alpha + \cos \alpha} \quad (8)$$

and

$$\frac{G_e}{\omega} = \frac{C_E}{\alpha} \cdot \frac{\sinh \alpha - \sin \alpha}{\cosh \alpha + \cos \alpha}, \quad (9)$$

where $\alpha^2 = 2\omega C_E R_S L_E^2 / A_E$ is a normalized relaxation frequency inversely proportional to the carrier transit time across the distance L_E , and C_E is the geometric capacitance of the area A_E of insulator covered by the excess semiconductor. Normally, the edge effect is a low frequency process and is well separated from the main relaxation which occurs when charge carriers in the semiconductor are unable to follow the applied signal voltage. The latter gives rise to the classic Maxwell–Wagner relaxation²⁸ which, for $R_I \gg R_B$, occurs at a frequency, f_B , given by

$$f_B = \frac{1}{2\pi R_B (C_I + C_B)}. \quad (10)$$

The dispersion caused by the series resistance, R_C , is generally centered at a frequency, f_C , well above the measurement range and is given by

$$f_B = \frac{1}{2\pi R_C} \cdot \frac{(C_I + C_B)}{C_I C_B}. \quad (11)$$

In the presence of a depletion region, C_I must be replaced by the series sum of C_I and C_D , the depletion region capacitance.^{11,25} However, the data in Fig. 4 do not support the presence of a conventional depletion region when V_G is below threshold. For example, according to the C - V plot in Fig. 3, the device is well into ‘‘depletion’’ when $V_G = 0$ V. Nevertheless, the low frequency capacitance continues to rise to ~ 146 pF, the value observed for accumulation voltages. If a siliconlike depletion region had formed, then the low frequency capacitance should saturate at a lower value corresponding to that observed in the C - V plot.¹¹ A similar upward trend in capacitance for decreasing frequencies also occurs for negative values of V_G . Furthermore, increasingly negative values of V_G do not reduce the low frequency capacitance to the value observed at high frequencies (~ 142 pF). Also for $V_G = 0, -10$ and -20 V, the capacitance plots merge into a single curve at ~ 10 kHz, again contrary to expectation for true depletion.¹¹

From the above observations, we conclude therefore that for these C_{60} devices, depletion is a consequence of reduced injection from the contact into the bulk semiconductor. Thus, the suite of Eqs. (5)–(9) can be used without modification to generate numerical fits to the data presented in Fig. 4. In attempting this seven-parameter fit, it should be noted that a given parameter set must simultaneously provide good agreement with both the capacitance [Fig. 4(a)] and loss [Fig. 4(b)] data. Furthermore, it would be expected that the values chosen for C_I , C_B , and C_E should remain essentially constant for all applied voltages. Within these constraints, the best fits that could be achieved are shown by the full curves in Fig. 4, which were generated using the parameter values given in Table I.

For $V_G > 10$ V, an excellent fit is obtained to the data and significantly better than could be obtained by ignoring the edge effect. For V_G below 10 V, the numerical curves reproduce the general features of the data but not the broad nature of the two main dispersions. Insofar as the edge effect is concerned, this is probably because of variations in the length, L_E , along the perimeter of the electrode. The broader

than the expected Maxwell–Wagner dispersion most likely arises from a frequency-dependent, hopping conductance in the C_{60} layer.

Notwithstanding these limitations, the numerical fits are illuminating. For example, from C_I we deduce that the capacitance per unit area, C_i , is ~ 1.6 nF/cm² and almost independent of V_G . Interestingly, the insulator resistance is much lower when the device is in accumulation, suggesting facile electron injection into the BCB. This is probably the origin of the slight hysteresis in the C - V plot in Fig. 3 when cycling V_G . The shift of the Maxwell–Wagner dispersion to higher frequencies is caused by a decrease in the resistance of the C_{60} layer from 220 to 75 Ω for increasing accumulation voltages. This is indicative of an increasing concentration of injected, extrinsic charge carriers (electrons) in the semiconductor at higher accumulation voltages. The capacitance, C_B , of the C_{60} layer decreases slowly with increasing accumulation voltages. The series resistance of the contacts is ~ 50 Ω and is probably associated with the short length of ITO track (~ 15 mm long \times 3 mm wide) between the contact point and the electrode itself. Finally, we note that the overall contribution, C_E , of the edge effect to the total capacitance is 2.44 pF ($=0.017C_I$) so that A_E is deduced to be 0.153 mm². Since the C_{60} layer overlaps the underlying gate stripe only on two sides, then $L_E = 25.5$ μ m. We note that the factor $R_S L_E^2 / A_E$ decreases by more than three orders of magnitude over the range -20 V to $+40$ V. This latter observation is easily explained by the shunting effect of the accumulation channel²⁵ on the sheet resistance of the excess “intrinsic” semiconductor (L_E in Fig. 5). This is confirmed in Fig. 2, where R_S^{-1} deduced from Table I scales remarkably well with the OFET mobility calculated from the transfer characteristics. From the above then, we may deduce that the 1.2 kHz C - V plot in Fig. 3, together with its associated maximum in loss, simply reflects the voltage dependence of the dispersion arising from the edge effect.

Although the above evidence is convincing, a voltage-dependent, low frequency dispersion, such as that attributed here to a parasitic effect arising at the perimeter of the MIS capacitor, can also arise from the tunneling of majority carriers into insulator trap states located close to the interface with the semiconductor.²⁹ Indeed, the slow increase in capacitance for decreasing frequencies when $V_G \geq 10$ V (semiconductor in accumulation) may well arise from such an effect. This being the case, additional elements of the form

$$C = \frac{qN_t}{2K} \left[\frac{\arctan(\omega\tau)}{\omega\tau} - \frac{\arctan(u)}{u} + \frac{1}{2} \ln \left(\frac{1 + \omega^2\tau^2}{\omega^2\tau^2} \right) - \frac{1}{2} \ln \left(\frac{1 + u^2}{u^2} \right) \right] \quad (12)$$

and

$$\frac{G}{\omega} = \left[\arctan(u) - \arctan(\omega\tau) - \frac{\ln(1 + u^2)}{2u} + \frac{\ln(1 + \omega^2\tau^2)}{2\omega\tau} \right] \quad (13)$$

should be included in the equivalent circuit. Here N_t is the volume density of insulator traps in a layer of width x at the

interface, K is a tunneling constant, and the parameter $u = \omega\tau e^{2Kx}$ where τ is a time constant given by $\tau = (\sigma_n v n_s)^{-1}$, where σ_n is the electron capture cross section, v is the thermal velocity, and n_s is the concentration of electrons on the semiconductor side of the interface. To study the effects arising from such a process requires MIS capacitors to be fabricated in which the edge effects believed to dominate in the present work are entirely eliminated.

IV. CONCLUSIONS

High mobility, n-channel OFETs based on highly crystalline C_{60} films deposited onto the insulator BCB have been fabricated. Classic capacitance-voltage plots obtained at 1.2 kHz from MIS capacitors show behavior normally associated with the formation of a depletion region in the semiconductor. However, even though the donor doping density extracted from the measurement is reasonable, the decrease in capacitance for depletion voltages arises from a different effect. This is confirmed by measuring the capacitance and conductance of the devices over a wide range of frequency and applied voltage. An equivalent circuit for the MIS capacitor is presented which accounts for well-recognized processes occurring in the bulk of the device. The circuit also includes a distributed RC network to account for the charging of additional insulator capacitance by lateral carrier transport through excess semiconductor protruding beyond the perimeter of the top contact. By fitting numerically generated plots based on the circuit, we provide evidence for the following:

- enhanced electron injection from the top contact into the C_{60} for increasingly higher accumulation voltages;
- a reduction in the insulation resistance of the BCB layer under accumulation voltages, presumably due to electron injection from the C_{60} layer; and
- a voltage-dependent dispersion associated with the perimeter of the capacitor that shifts to higher frequencies as the gate voltage moves through the range -20 to 40 V. It is this dispersion that gives rise to the observed C - V and G/ω - V plots rather than a conventional depletion region with interface states.

Furthermore, our results suggest that the threshold voltage of the OFETs is related to the injection of extrinsic charge carriers into the semiconductor and that the sub-threshold region and “off” state of the transistor reflect reduced electrode injection rather than the formation of a space-charge layer of ionized dopants.

While the evidence presented strongly supports the presence of a parasitic edge effect, tunneling of electrons from C_{60} into insulator states could give similar behavior and cannot definitively be ruled out.

Finally, this study has shown that the unambiguous interpretation of C - V data requires supporting evidence from admittance spectroscopy. It has also been demonstrated that care is required when designing and fabricating MIS devices if artifacts connected to parasitic effects are to be avoided.

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