Interfaces and traps in pentacene field-effect transistor

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The equivalent circuit parameters for a pentacene organic field-effect transistor are determined from low frequency impedance measurements in the dark as well as under light illumination. The source-drain channel impedance parameters are obtained from Bode plot analysis and the deviations at low frequency are mainly due to the contact impedance. The charge accumulation at organic semiconductor–metal interface and dielectric–semiconductor interface is monitored from the response to light as an additional parameter to find out the contributions arising from photovoltaic and photoconductive effects. The shift in threshold voltage is due to the accumulation of photogenerated carriers under source-drain electrodes and at dielectric–semiconductor interface, and also this dominates the carrier transport. The charge carrier trapping at various interfaces and in the semiconductor is estimated from the dc and ac impedance measurements under illumination.
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I. INTRODUCTION

Considerable interest in organic field-effect transistors (OFETs) based on small molecules, polymers and composites have emerged in past few years due to the low cost of fabrication, ease of processing and mechanical flexibility.[1–3] Organic semiconductors can be processed from solution at room temperature and printed onto a variety of flexible substrates. Although the device performance of OFETs is typically lower than that of inorganic counterparts, printed electronic circuits using OFETs may become viable alternative to silicon based systems, especially in large-area applications.[4,5]

Pentacene, a member of the oligoacene family, stands out as an attractive candidate for OFET applications on account of its relatively high charge carrier mobility of the order of 1 $cm^2/V\,s$.[6] The electrical characteristics of the devices are dominated by the interface between pentacene and gate dielectric, and also the interfaces with source and drain metal contacts. Various phenomena like energy level alignment, dipole layer formation and band bending in the organic layers occur at the interfaces that often create injection barriers, relevant for the FET operation. In the source-drain (SD) electrodes–semiconductor interface, contact resistance affects the carrier injection and low barrier height is preferred.[7] As the device dimension decreases, the contact resistance as a part of the total device resistance will dominate over the channel resistance, and thereby limiting the transport in OFETs which determine the speed of organic integrated circuits, then the role of intrinsic carrier mobility of organic semiconductor becomes less dominant.[8] The dependence of contact resistance in top-contact (TC) and bottom-contact (BC) geometrical configurations of pentacene OFET shows that TC-OFETs offers lower resistance because of the increased area of contact.[9] The TC-OFETs have superior performance and ease of fabrication but lacks suitable procedure to pattern the FET active layer to isolate the devices from each other.[10] In BC-OFETs, drain and source contact metal is deposited on the gate dielectric and patterned prior to the active layer deposition. In this geometry the source and drain series resistance are nonlinear, especially affecting the transport at low V_{DS}.[10,11] Hence optimization of the interface between SD electrodes and organic semiconductor along with the gate dielectric–semiconductor interface are the important factors to enhance the OFET performance. Soft contact lamination of SD electrodes by gold-coated high-resolution rubber stamps on the organic semiconductor films showed improved performance as the mechanical conformability is enhanced and the chemical modifications are lowered.[12] Further, doping the semiconductor at source drain contact interfaces has reduced the contact resistance to some extend.[13] However, a detailed characterization of the interfaces are yet to be carried out to improve the overall performance of OFETs.

The performance of OFETs depends crucially on the use of dielectrics which form active interfaces with the organic semiconductor. The ON or OFF states of an OFET is determined by the presence or absence of gate-induced charge at the semiconductor–dielectric interface.[14] The structural and electrostatic disorder in the first few layers of the organic semiconductor next to the insulator cause undesirable effects like lowering the OFET ON current, reduction in the switching speed, hysteresis, and increase in the threshold voltage.[14,15] Hence it is possible to alter the threshold voltage in organic transistors by controlling the density of semiconductor–dielectric interface states. The large mobility values and high on-off ratios result from a reduction in the number of scattering/trapping sites at the interface between the semiconductor and insulator.[15] Further charge trapping effects at the semiconductor–dielectric interface can lead to hysteresis which is commonly observed for OFETs and is sweep rate dependent. Hysteresis can be eliminated by slowing down the sweep rate but practical applications need fast

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sweep rate.[11,15] Hysteresis can lead to apparent gate voltage dependence for mobility, deviation of threshold voltage and an apparent lack of saturation for output curves[11] and hence should be preferably minimized for many conventional applications except nonvolatile memory applications of OFETs.[16,17] The traditional material used as dielectric is silicon dioxide (SiO_2). Despite a number of excellent properties, SiO_2 suffers from a relatively low dielectric constant ($k=3.9$). The major motivation to search for SiO_2 alternatives is to substantially reduce the OFET operating voltages.[3] Moreover low polarity at the dielectric–semiconductor interface is desirable as it increases the carrier mobility.[18] Organic dielectrics are used as an alternative to the inorganic ones, since organic dielectrics can be solution processed, can possess a rather high dielectric constant, provides smooth films on plastic substrates and glass; and suitable in optoelectronics as the optical transparency is high, with thermal stability upto 200 °C.[15] However, the choice of organic dielectric affects the OFET performance.[19] Moreover, growing the organic film on gate dielectrics with different dielectric constant and surface energy shows a wide variation in morphology.[19–21] Apart from the contact interfaces and semiconductor–dielectric interfaces, grain boundaries also play an important role in determining the electrical properties of polycrystalline thin films. The presence of inhomogeneous carrier traps in pentacene has been reported by measuring the potential profile.[22] It has been suggested that the sites in polycrystalline pentacene near the gate dielectric and also the grain boundaries act as carrier traps.[22] More recently it has been reported that in very thin pentacene films with island morphology charge trapping occurs primarily in the intergrain regions between the pentacene islands.[23]

Several methods have been employed to evaluate the contact resistance and among them transfer linear method developed from amorphous silicon FET theory is traditionally used. In this method, the total resistance (contact +channel) is measured as a function of the channel length, by making multiple FETs with various channel lengths. The channel resistance is proportional to the channel length. The contact resistance can be extracted from the total resistance by extrapolating for zero-length channel since the contact resistance is assumed to be independent of the channel length.[24] A modified atomic force microscopic (AFM) measurement to investigate the surface potential as a function of the position across the biased channel has been reported by Seshadri and Frisbie.[25] In this method a high impedance electrometer is used to sense the potential of a metal-coated AFM tip when it comes in contact with discrete points across the channel. The AFM potential profile measurement on a sexithiophene OFET suggested that the maximum drop takes place across the source and drain rather than along the channel.[25] However, the contact AFM technique is potentially destructive and unable to profile the potential of active material buried below the gate dielectric media. Instead a noncontact potentiometry technique Kelvin probe force microscopy (KFM), can be used to map the potential profile across the operating FETs.[26] This measurement technique relies on estimating the potential profile from the capacitive forces on an electrically excited cantilever, which depends on the surface potential.[26–28] Moreover in this measurement it is the interfacial potential (i.e., potential across the accumulation layer) that is mapped and not the surface potential.[26] The charge transport bottlenecks in OFETs can be identified from the sharp voltage drops in the potential profile. Furthermore the correlation between the potential and surface morphology can be studied from KFM measurements. Recently, a number of new AFM (both contact and noncontact) techniques have been developed to probe the role of interfaces in carrier generation, and to correlate local variations in morphology with macroscopic device performance.[29] A relatively simple gated four-probe technique involving the sensing of potential between two points between source and drain has also been used for estimating the contact resistance.[30] Using this method it is possible to measure the temperature-dependence without requiring the sophistication of a UHV-AFM system, even though this approach does not provide the details obtainable from KFM technique. Nevertheless, the scanning probe techniques to map the potential profile has limitations in probing the capacitive contributions arising from the charge trapping and accumulation in interfaces and bulk, which often play a significant role in the device response.

Impedance characterization of these devices can provide insight into the transport mechanism occurring at bulk and interfaces, and from this the circuit elements can be identified.[31,32] However, only a few results have been reported so far on the ac impedance analysis of OFETs under dc bias conditions,[31,32] while the dc characteristics have been widely investigated in this field. Since many organic materials used in FETs have a good photosensitivity, the photoimpedance measurements can give a detailed understanding of the carrier generation, mobility and trapping related properties.[33,34] The KFM measurements in the presence of light are limited to probe a few semiconductor monolayers at the interface of the gate dielectric.[35] The ac and dc characterization of OFET in presence and absence of light and equivalent circuit modeling are quite essential to distinguish the charge transport properties of the device due to various contributions arising from gate dielectric–semiconductor interface, contact effects and the grain boundary effects. Although the dc resistive response in KFM measurements provides the information about dielectric–semiconductor interface and grain boundaries, the ac impedance data are required to investigate the capacitive contributions, especially to distinguish the traps at the bulk and interfaces.[32] From later, an estimation of the carrier accumulation and trapping at various interfaces and bulk semiconductor can be determined as shown below. Such an investigation can help to identify the operational bottlenecks and to improve the performance of OFETs in light detectors and optical switches.[11]

In this work, we present the low frequency impedance measurements across the SD terminals of a pentacene OFET under dc bias and under light illumination along with the dc characteristics under illumination. The results from these measurements have assisted to find the equivalent circuit of the OFET. The numerical response based on these parameters shows deviation at low frequency, which is related to the charge accumulation and the contact resistance and ca-

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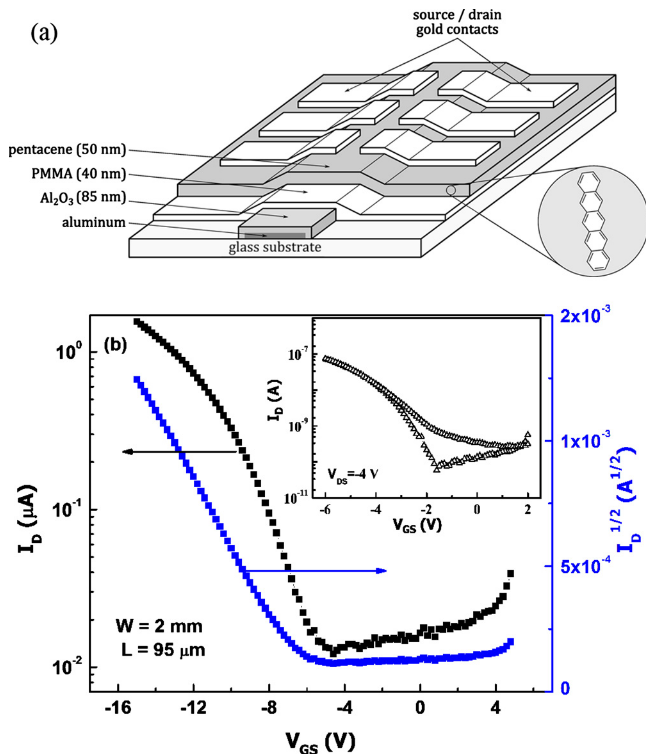

FIG. 1. (Color online) (a) Schematic diagram of the pentacene OFET. (b) Transfer characteristics of pentacene OFET in dark. Inset shows the hysteresis in the transfer characteristics.

pacitance at the interfaces. The dc photoresponse shows shift in threshold voltage which is attributed to the charge accumulation at the contact and dielectric–semiconductor interfaces and the charge accumulation at the dielectric–semiconductor interface is estimated. From these ac and dc measurements it is possible to obtain a quantitative estimation of the resistive and capacitive contributions occurring at the bulk and interfaces of OFETs.

II. EXPERIMENTAL

The pentacene OFETs are fabricated in the bottom-gate, TC configuration, as schematically depicted in Fig. 1(a). For the device fabrication, aluminum (150 nm) is evaporated on glass and then partly oxidized electrochemically at a constant current density of 0.6 mA cm^{-2} in 0.01 M citric acid solution.[36] The oxidation is stopped when the layer thickness exceeds 85 nm. The alumina layer thickness is checked using capacitance and cross-section scanning electron microscopy (SEM) measurements. After rinsing the oxide and treating it with water at 80 °C, it is dried in vacuum at 150 °C. Poly-(methyl methacrylate) (PMMA) (Aldrich, M_w=996 000 GPC) is used to passivate the oxide-surface,[37] therefore a 40 nm layer of PMMA (100 ppm solution in acetone) is spun at 1500 rpm. This dielectric bilayer exhibits a geometrical capacitance of 35 nF cm^{-2} with a breakdown voltage in the range of 5 MV cm^{-1}. Further PMMA gate dielectric helps in minimizing the hysteresis due to the charge trapping at the dielectric–pentacene interface.

Pentacene (purchased from Aldrich and cleaned in a further sublimation step) is evaporated on top of the dielectric at 0.5 Ås^{-1} rate, and at a substrate temperature of 50 °C in a hot wall epitaxy system.[38] 70 nm gold SD contacts are evaporated using a shadow mask, with 95 μm channel length (L) and 2 mm channel width (W), to complete the fabrication of the transistor, and ready for the complementary electrical and optical characterization.

The *I-V* characteristics of the devices under applied gate voltage were measured using Keithley Sourcemeters (Model Ke-2400 and Ke-2611). The measurements were performed in a Janis continuous flow optical cryostat under 10^{-2} Torr vacuum to avoid exposure to ambient conditions. A lock-in amplifier based technique was used to find the low frequency ac impedance across the SD channel of the OFET. An appropriate dc bias (V_{DS}) together with a superposed ac small signal (50 mV) is applied across the SD electrodes of the OFET and the complex ac voltage responses are measured using a lock-in amplifier (SR-830) and a resistor-divider as described elsewhere.[31] Further, the pentacene OFET was characterized under monochromatic light irradiation at a wavelength of 532 nm using a diode laser (Model Roithner-Lasetechnik) and the corresponding values of the impedance are also measured. The devices were stable during the measurement interval under illumination, and bias-stress degradation effects were negligible.[39]

III. RESULTS AND DISCUSSIONS

The transfer characteristics of the pentacene OFET is plotted in Fig. 1(b). The room temperature on-off ratio is found to be 200. The mobility is calculated in the linear regime, using the relation:

$$I_{DS} = \mu \frac{W}{L} C_i (V_{GS} - V_T) V_{DS}, \tag{1}$$

where μ is the mobility, C_i is the capacitance per unit area of the gate dielectric, V_T is the threshold voltage, and W, L are the channel width and length, respectively. The mobility at room temperature is ~0.08 cm^2/V s. The OFETs showed negligible hysteresis in the transfer characteristics [see Fig. 1(b) inset]. This weak hysteresis indicates that a significant number of traps are in the shallow levels, and in case of deep level traps the hysteresis is expected to be larger; however, this needs more detailed investigation in future.

In Fig. 2(a), the transfer curves (V_{DS}=−8 V) of the pentacene OFET in the dark and under a monochromatic light (532 nm) of various intensities are presented. The absorption spectrum of evaporated pentacene of 50 nm thickness is shown in the inset of Fig. 2(a). Pentacene is excited at 2.33 eV that is above the transport gap at 2.2 eV. The photogeneration causes the increase in the drain current, e.g., by a factor of 22 at 2 mW/cm^2 light intensity. In the experiments, the light intensity was varied from 0.4 to 16 mW/cm^2. Large number of excitons, subsequently electrons and holes, are generated when photons of energy equal to or higher than the band-gap are absorbed, and this causes the increase in drain current. As the illumination intensity is increased, the drain current also increases, since the number of photogenerated carriers increases with the intensity of light.[34] Alongside with the gate bias the effect of light offers an additional control for the charge carrier generation in the

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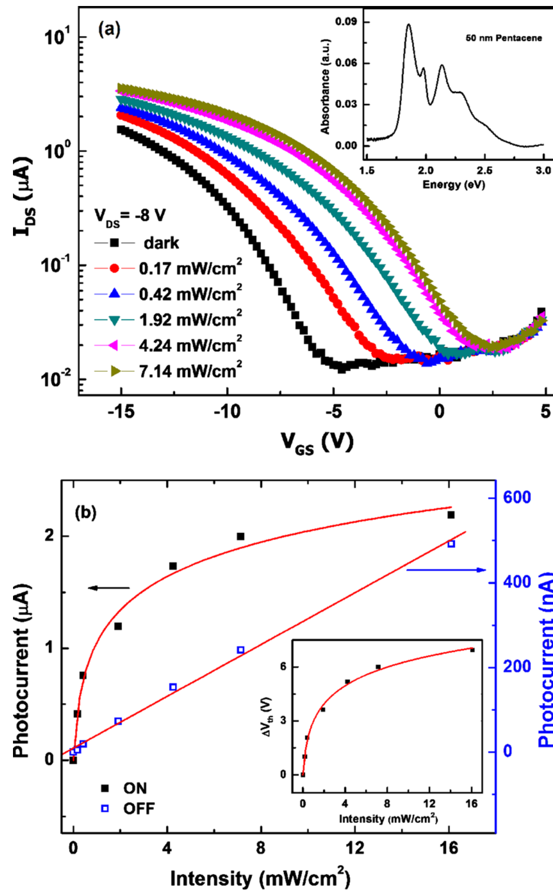

FIG. 2. (Color online) (a) Transfer characteristics of pentacene OFET in the dark and under illumination at various intensities. Inset shows the absorption spectrum of pentacene (50 nm thick film). (b) Photocurrent as a function of incident light intensity under turn-on and turn-off states. Solid lines are fits to Eqs. (2) and (3). Inset: threshold voltage shift vs light intensity.

transistor.[33] The photoinduced response of the OFET is explained in terms of photoconductivity and photovoltaic effects. Photoconductivity effect causes an increase in the drain current when the OFET is in the off state, whereas photovoltaic effect is responsible for the shift in its switch-on voltage (V_{on}) and threshold voltage (V_T), under illumination.[40] When the OFET is in the off state, the increase in current is relatively small with the optical power, and the photocurrent is expressed by the linear relationship[41]

$$I_{ph,pc} = (q\mu_p pE)WD = BP_{opt}, \tag{2}$$

where p is the carrier density, E is the electric field in the channel, W is the gate width, D is the depth of absorption region, P_{opt} is the incident optical power, and B is a proportionality constant. The photocurrent in the off state is therefore directly proportional to the incident light intensity, as shown in Fig. 2(b).

When the device is in the on state, the photovoltage induced by the accumulation of large number of electrons under the source electrode or at the interface between the semiconductor and gate dielectric gives rise to a significant increase in current. Among the photogenerated carriers in the pentacene channel, produced by the absorption of light, holes easily flow to the drain electrode due to higher mobility, whereas electrons accumulate under the source electrode or at the gate dielectric due to the lower mobility.[34] These accumulated electrons effectively lower the potential barrier between the source and the semiconductor channel, leading to a shift in the switch-on voltage and threshold voltage, as shown in Fig. 2(a).[40] The shift in switch-on voltage (V_{on}) suggests that more number of photogenerated carriers are being trapped at the interfaces. The shift in threshold voltage (ΔV_T) toward positive voltages shows logarithmic variation with light intensity as shown in the inset of Fig. 2(b), and this is in agreement with model used in the data analysis as in Eq. (3). The photocurrent caused by photovoltaic effect is given by the following expression:[42]

$$I_{ph,pv} = G_M \Delta V_T = \frac{Ak_BT}{q}\ln\left(1 + \frac{\eta q \lambda P_{opt}}{I_{pd}hc}\right), \tag{3}$$

where η is the quantum efficiency, q is the elementary charge, I_{pd} is the dark current for electrons, hc/λ is the photon energy, G_M is the transconductance, ΔV_T is the threshold voltage shift, and A is a fitting parameter. The photocurrent as a function of incident optical intensity under the turn-on ($V_{GS}=-12$ V) and turn-off ($V_{GS}=-1.5$ V) states at $V_{DS}=-8$ V is shown in Fig. 2(b). The fit to the data for the turn-off condition shows a linear dependence, whereas the turn-on condition clearly shows the characteristic logarithmic behavior, as given by Eq. (3).

The threshold voltage can be associated with the charges trapped in interface states and the injection barrier at source electrode; and it is possible to estimate the upper limit for the density of hole trapping interface states N_I from[43]

$$N_I = \frac{-Q_I}{e} = -\frac{C_i}{e}[V_T - (\Phi_m - \Phi_S) + V_{inj}] \leq -\frac{C_i}{e}V_T, \tag{4}$$

where $(\Phi_m - \Phi_S)$ is the difference between gate and organic semiconductor workfunctions, Q_I is the trapped charges in the interface states at the semiconductor-dielectric boundary, and V_{inj} is a term that depends on the injecting contact. A surface charge density of 1.9×10^{12} cm^{-2} accounts for the observed threshold voltage (~ -8.6 V) in the dark.[43] However, the actual value of N_I can be smaller. Upon illumination, the threshold voltage shifts toward positive voltages and the increase in carrier density can be estimated from: $\Delta N_I = C_i \Delta V_T / e$. The charge accumulation at various light intensities is presented in Table I.

The impedance characterization of these devices under dc bias and under light illumination is essential for a comprehensive understanding of the equivalent circuit, and to develop theoretical models for injection and transport in organic devices. Usually Bode plot analysis is being carried out to understand the ac response of the FET.[31] The phase value (φ_0) is plotted as a function of frequency in Fig. 3(a) and the magnitude of the complex SD channel impedance Z_O, represented in units of decibels, is plotted as a function of log f in Fig. 3(b), for different intensities of incident light and also under dark condition. The negative phase angle increases in magnitude while increasing the frequency. The high frequency asymptote has a slope of nearly −20 dB/decade, as known in linear time-invariant system that follows

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TABLE I. The charge accumulation and trapping parameters for pentacene OFET under various light intensities. [ΔQ_{B0} and ΔQ_{C0} are the small-signal differential charge accumulated in the channel and at the MS contact interface, respectively, in the dark. Q_{I0} ($\sim 1.9\times 10^{12}$ cm^{-2}) is the charge accumulated at the gate dielectric–semiconductor interface in the dark.]

Intensity (mW/cm^2)	ω_c (kHz)	R (MΩ)	C (pF)	Charge trapping in the bulk ($\Delta Q_B/\Delta Q_{B0}$)	Charge accumulation at the MS contact interface ($\Delta Q_C/\Delta Q_{C0}$)	Charge accumulation at the gate dielectric interface (Q_I/Q_{I0})
Dark	0.48	1.00	332	1	1	1
0.42	0.72	0.45	492	1.04	1.34	1.24
1.9	0.91	0.27	648	1.09	1.75	1.42
4.2	1.21	0.15	877	1.16	2.23	1.63

the first order ordinary linear differential equation. For such systems, the transfer function in polar form is as follows:[31]

$$|G(\omega)| = \kappa/[1+(\omega/\omega_c)^2]^{1/2}, \quad (5)$$

$$\varphi_O(\omega) = \tan^{-1}(-\omega/\omega_c), \quad (6)$$

where κ and ω_c are system dependent constants. The corner frequency ω_c is determined by plotting φ_0 versus ω (or f) and from such a plot the value of ω_c at $\varphi_0=45°$ [see Eq. (6)] can be obtained. Substituting the values for ω_c and $|G(\omega_c)|$ in Eq. (5), the value of κ can be estimated. Thus Bode plots can be used to determine the system dependent constants, κ and ω_c, in the analysis of the equivalent circuits of OFETs.

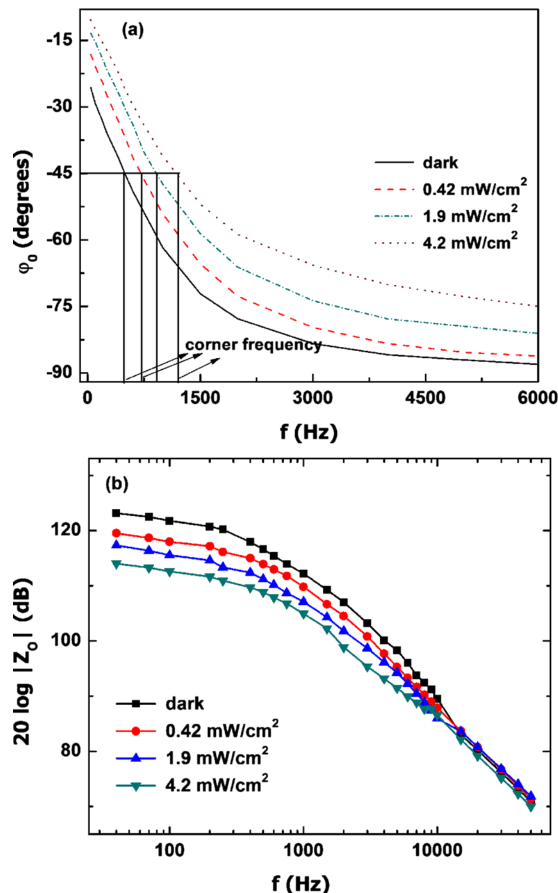

FIG. 3. (Color online) (a) Phase vs frequency. The corner frequency (f_c) is the frequency value at −45°. (b) Bode plot of output impedance for pentacene OFET.

The ac equivalent circuit of the SD channel is determined from the complex form of impedance expressed in terms of complex current $I(\omega)$ and voltage $V(\omega)$, which is expressed as,

$$I(\omega) = (1/\kappa)V(\omega) + j\omega[1/(\kappa\omega_c)]V(\omega). \quad (7)$$

Equation (7) resembles the sum of current passing through a parallel network of R and C with $R=\kappa$ and $C=1/(\kappa\omega_c)$. Using these values and Eq. (5), the numerical form of $|Z_O(\omega)|$ can be generated and is plotted with experimental data under dark and at various light intensities, as in Fig. 4. The numerically simulated curve matches with the measured data, except at low frequencies. Table I summarizes the equivalent circuit parameters of pentacene OFET at various light intensities. The low frequency deviations to the channel impedance are possibly due to the contributions from contact resistance (R_c) and contact capacitance (C_c) and the deviations are modeled with additional parallel R_c-C_c element in series with the output resistance R as shown in the inset of Fig. 4.[31,32]

The significant contact resistance observed in pentacene OFET can be due to the injection barriers at the contacts or due to the presence of trap states at the metal-semiconductor (MS) interface.[30] The direct evaporation of gold on pentacene thin film to form source and drain contacts, cause dif-

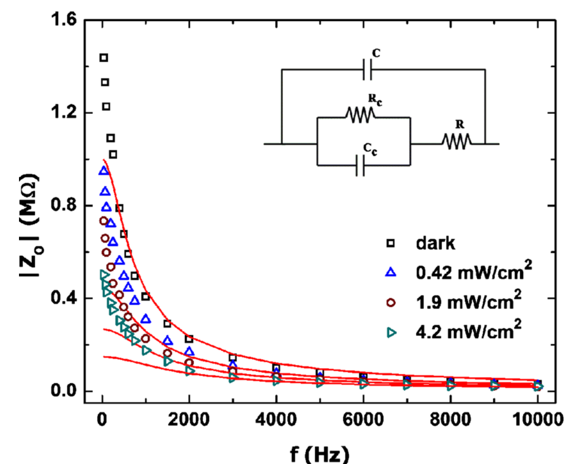

FIG. 4. (Color online) Output impedance $|Z_O|$ vs frequency for pentacene OFET in the dark and under monochromatic light of various intensities. Solid lines are the simulated curves from equivalent circuit parameters. Inset shows the equivalent circuit.

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fusion of gold into the pentacene and create contact interface traps sites. Further the presence of moisture and grain boundaries at the drain and source contact interfaces may also lead to trapping of carriers.[44] Illumination enhances the trapping process by providing more number of electrons. In general the trapping of carriers occurs at MS contact interfaces, trap states present in the semiconductor channel itself and at the semiconductor–gate dielectric interface. Usually this increase in the trapping process in OFETs under light illumination is indicated from the shift in threshold voltage in the dc transfer characteristics.[40] However, this cannot distinguish the contributions arising from various interfaces and the traps present in the bulk semiconductor.[32] Nevertheless this can be estimated more accurately from the impedance measurements as in this work. The applied ac voltage drops across the MS interfaces and also the active semiconductor channel. The ratio of the ac voltage drop across the MS interface and SD-channel is determined from the ratio of low frequency impedance deviation (which represents the interface drop) to the simulated curve (which represents the channel drop).[32] This voltage drop, combined together with the contact capacitance, yields the small signal differential charge (ΔQ) accumulated at the MS interface, as shown in Table I. This small-signal differential charge is the charge added/ subtracted from the total charge in response to the ac voltage applied under dc bias in the low frequency limit, and this increases with illumination under constant bias conditions.[32] Under the effect of illumination, the ac voltage transfers more charge to the interface and the possibility to get trapped there is also larger. Under the illumination of light of intensity 4.2 mW/cm^2, the trapped charges at the MS interfaces increases by a factor of ~ 2.3 and it increases by a factor of ~ 1.63 at the gate dielectric–semiconductor interface, which is an evidence for the charge accumulation phenomenon in the photovoltaic regime. In addition to this, the SD channel capacitance C also increases with light intensity, which is due to the trapping of photogenerated carriers in the bulk of the polymer. In this way the trapping processes occurring in the bulk and interfaces can be distinguished. The trapping of photocarriers in the bulk of the polycrystalline pentacene is occurring mainly at the grain boundaries. However the significant accumulation of photogenerated carriers is observed at the MS contact interfaces and at the semiconductor–gate dielectric interface which limits the charge transport in pentacene OFET. These results suggest that the roles of MS contact and semiconductor–dielectric interfaces have to be understood in detail to improve the performance of OFETs.

IV. CONCLUSIONS

In summary, the charge accumulation and trapping in pentacene OFET have been determined from the dc and ac impedance measurements. The photoresponse studies could sensitize in quantifying the accumulation and trapping processes in the OFET. The ac equivalent circuit parameters of the SD channel for pentacene OFET is determined under dark and at various light intensities. The photoresponse characteristics are dominated by the photoconductive (turn-off state) and photovoltaic (turn-on state) effects. The equivalent circuit parameters obtained show that the channel resistance decreases by almost an order of magnitude and the channel capacitance increases by almost a factor of three under light illumination, which is mainly due to the photogeneration and trapping of carriers. The contact impedances are observed to be contributing to the low frequency deviations. The determination of the equivalent circuit in presence and absence of illumination can quantify the small-signal differential charge added/subtracted from the total charge accumulated at MS interface. The trapping of charge carriers at dielectric–semiconductor interface is estimated from the threshold voltage shift under illumination. The accumulation/trapping of charge carriers at various interfaces and at grain boundaries within the channel are summarized in Table I. A significant accumulation of photogenerated carriers is observed at the MS contact interfaces and at the semiconductor–gate dielectric interface which limits the charge transport in pentacene OFET. Such an investigation is useful to identify both the carrier transport and trapping mechanisms in OFETs.

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