Electrical properties of pSi/[6,6] phenyl-C61 butyric acid methyl ester/Al hybrid heterojunctions: Experimental and theoretical evaluation of diode operation

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(Received 29 October 2012; accepted 1 November 2012; published online 5 December 2012)

In this work, we analyze electrically the Al/p-Si/[6,6] phenyl-C61 butyric acid methyl ester/Al hybrid heterojunction. The barrier height at the p-Si/PCBM interface corresponding to the difference between Si valence band edge and the lowest unoccupied molecular orbital energy level of PCBM is studied with current-voltage (J-V) and capacitance-voltage (C-V) methods and determined to be $\simeq 0.55$ eV. This value is in agreement with the onset energy of spectrally resolved photocurrent measurements presented in a previous publication [Matt *et al.*, Adv. Mater. **22**, 647 (2010)]. For the J-V characteristics, a thorough model based on an interface generation-recombination current is proposed. All relevant energy levels for this model are obtained experimentally. As origin of the large reverse current, the thermal generation of charge carriers throughout the Si depletion region is identified by the thermal activation measurements. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4768271]

I. INTRODUCTION

In the last decade, the technology of organic semiconductors has made a huge step towards a large-scale industrial production and the presence in the major markets. Simultaneously, the field of hybrid organic/inorganic devices has been studied.[1] Hybrid devices combine low-cost, large-area processability of inherently cheap, ubiquitous, potentially environmental sustainable materials, with the compatibility with the well established silicon CMOS technology.

In our previous work, we have reported the photocurrent generation in the mid- and near-infrared spectral region with inorganic/organic hybrid heterojunctions based on p-Si and fullerene.[2] Fullerenes and their derivatives constitute a very special case of organic compounds which can possess semiconducting, metallic[3,4] and even superconducting properties.[5] Due to the large energy gap of fullerenes between the lowest unoccupied molecular orbital (LUMO) and the highest occupied molecular orbital (HOMO), almost no free charge-carriers are available for transport at ambient temperatures.

The first hybrid silicon/fullerene heterojunctions were presented in the early 90 s exhibiting rectification on both n- and p-type Si substrate,[6,7] probably due to non-perfect purity of the material in the early years of C_{60} industrial production. Further attempts focused on p-Si/C_{60} hetorjunctions applied as a photovoltaic device aiming at the extension of light harvesting spectra.[8,9] However, none of the cited publications presented a comprehensive model for the diode operation, adapting rather the classic diode equation in the form of Schottky formula.

In this work, we present a detailed theoretical model for the diode operation based on recombination-generation mechanism given by Shockley and Read[10] supported by the experimental results of capacitance-voltage (C-V) and temperature dependent current density-voltage (J-V) analysis.

II. EXPERIMENTAL

The Al/p-Si/PCBM/Al heterojunction was fabricated on $15 \times 15\,mm^2$ p-type Boron doped (100) silicon wafer-piece (doping concentration $N_A \sim 2 \cdot 10^{15}\,cm^{-3}$) by spin coating of the soluble C_{60} derivative methano-fullerene [6,6] phenyl-C61 butyric acid methyl ester (PCBM) purchased at Solenne BV Netherland. Prior the organic layer deposition, the Si substrate was initially chemically cleaned using the RCA[11] cleaning procedure consisting of: base bath (1:1:5 solution of $NH_4OH/H_2O_2/H_2O$) for removal of organic contaminants, oxide strip (5% HF) for removal of the native oxide, and acid bath (1:1:5 solution of $HCl/H_2O_2/H_2O$) for removal of ionic contamination. Afterwards, the sample was transferred to the vacuum chamber of a physical vapor deposition (PVD) system for depositing an 80 nm thick Al film. To provide ohmic contact to the p-Si substrate, the sample was heated to 580 °C in 10:1 N_2/H_2 reducing atmosphere of an annealing system to form a Si/Al alloy in the contact region.[12,13] Thereafter, the sample was cleaned again by a RCA procedure and transferred to a glove box system with N_2 atmosphere (O_2 contents below 1 ppm) within less than a minute to suppress the formation of native SiO_2 on the p-Si substrate. Based on this process, no indications of device failure due to the presence of a native SiO_2 layer were found.

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In the glove box, a PCBM solution (3 wt. % in chlorobenzene) was spincoated on top of the cleaned p-Si substrate. Finally, PCBM top contacts with areas of 14 mm^2 were fabricated by thermal evaporation of Al using a PVD system directly accessible from within the glove box, thereby preventing oxygen diffusion into the PCBM thin film. The finished devices were contacted by conductive silver paste and mounted into sealed measurement containers in the N_2 atmosphere of the glove box system. The PCBM film thickness was measured with atomic force microscopy on a reference sample. The device fabrication process was optimized for a PCBM layer thickness of $\simeq 165$ nm, since for this thickness the maximum responsivity was observed when the devices were operated as photodetectors in the telecom wavelength region.[2]

III. RESULTS AND DISCUSSION

Figure 1 shows the current density vs voltage (J-V) characteristics of heterostructure diodes measured at 300 K. In this plot, the results obtained from sixteen devices fabricated in five batches are summarized. From each batch, devices with the largest rectification ratio [defined as J(1 V)/J(−1 V)] were chosen in order to minimize the influence of devices degraded by process defects on the data set. Throughout the paper, data shown by blue symbols in Figs. 1 and 2 were obtained from one and the same particular device. The data spread obtained from all investigated devices is indicated by the error bars in Figs. 1 and 2, the length of which corresponds to the difference between maximum and minimum data values.

For a bias variation from −1 to +1 V, a current rectification ratio of 0.7×10^4 is observed. The rectifying behavior of J-V characteristics indicates directly the presence of a barrier for the charge carriers. As has been pointed out in our previous work,[2] both metal contacts are ohmic and the barrier is formed at Si/PCBM interface.

The barrier height was determined by the C-V experiments in which the capacitance has been recorded at frequency 1 kHz with 5 mV modulation voltage. Figure 2 shows a nearly linear dependence of $1/C^2$ on the bias voltage.

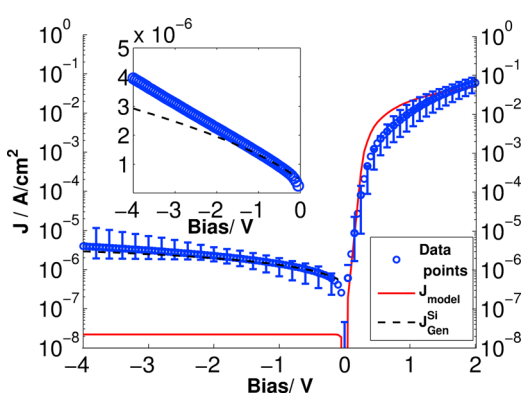

FIG. 1. J-V characteristics of Al/p-Si/PCBM structure. The results of the modeling using the ideal interface generation-recombination model (Eq. (3)) including parasitic series resistance are shown by the red line. The error bars are calculated from data of sixteen diodes as discussed in the text. Inset: J-V in reverse direction in linear scale. The results of modeling the J-V characteristics using space charge region generation are shown by the broken black line.

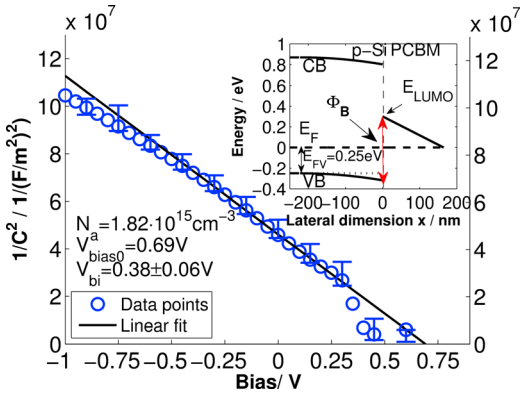

FIG. 2. $1/C^2$ vs V characteristics of Al/p-Si/PCBM/Al heterojunction diodes. The length of the error bars corresponds to the difference between maximum and minimum data values obtained from nine diodes fabricated in two different batches with the same parameters. Inset: Schematic picture of band alignment at the interface for short circuit condition. All values are in scale and have been calculated from the Poisson's equation. E_F is the Fermi level, which is constant throughout the bulk of the device for equilibrium condition. The HOMO level of PCBM is not shown for the sake of clarity.

To estimate the built-in potential and subsequently the barrier height of the investigated heterojunction from C-V measurement, we assume that at reverse bias a depletion layer and, thus, a space charge builds up in the Si and that no localized charges are present in the PCBM layer. The charge complementary to the one stored in the Si space charge region is, thus, exclusively located at the metal contact to the PCBM layer.

From the solution of Poisson's equation for the space charge profile defined above, the following expression for $1/C^2$ results:

$$\frac{1}{C^2}(V_{bias}) = \left(\frac{d}{\varepsilon_0 \varepsilon_{C60}}\right)^2 + \frac{2(|V_{bi}| - V_{bias})}{|q|\varepsilon_0 \varepsilon_{Si} N_A}. \qquad (1)$$

Here, d is the thickness of the PCBM layer, $\varepsilon_{Si} = 11.7$ and $\varepsilon_{C60} = 3.9$ are the relative dielectric constants of silicon and PCBM. N_A, V_{bias}, q, and ε_0 denote the acceptor doping concentration in the Si, the externally applied voltage, the electric charge, and the vacuum dielectric constant, respectively. The built-in potential V_{bi} is the voltage drop across the device at $V_{bias} = 0$ which results as a consequence of the equilibrization of the electrochemical potential across the device. The band edge profiles obtained from solving Poisson's equation for $V_{bias} = 0V$ are shown in the inset of Fig. 2. They exhibit a bending on Si side due to a space charge layer and a constant decay due to a constant electric field in the PCBM layer.

Equation (1) predicts a linear dependence of $1/C^2$ on V_{bias} in excellent agreement with the experimental data shown in Fig. 2. In this plot, the data spread indicated by the error bars is obtained from C-V measurements on nine devices. The small deviation from the linear behavior at large negative bias (i.e., at small junction capacitance) is attributed to stray capacitances in parallel with the device. Based on the data of nine samples fabricated in two different batches fabricated under nominally the same conditions, from the slope obtained for small voltages (shown by the solid line in

Fig. 2), an average value of a Si doping concentration of $N_A = 1.82 \cdot 10^{15}\,\mathrm{cm}^{-3}$ is determined in excellent agreement with the wafer specifications. From the intersection of the linear fit with the abscissa axis in Fig. 2, the average built-in potential $V_{bi} = 0.38 \pm 0.06$ V is calculated. The uncertainty mainly results from the uncertainty of the PCBM layer thickness as calculated from the statistical error propagation law[14] using Eq. (1). From the standard deviation ($\sigma = 0.04$ eV) of the V_{bi} values obtained from nine different samples, we conclude that the influence of uncontrolled impurities on the Si substrate surface and/or native SiO_2 layers do not significantly contribute to the total uncertainty (0.06 eV) of the determined V_{bi} value. From V_{bi}, the average barrier height $\Phi_B = 0.63 \pm 0.06$ eV can be calculated according to[15]

$$\Phi_B = E_{LUMO}^{x=0} - E_{VB}^{x=0} = |q|V_{bi} + E_{FV}. \tag{2}$$

Here, $E_{FV} = kT\ln(N_V/N_A)$ is the energy difference between Fermi level and the Si VB outside the depletion region, and $N_V = 2.66 \cdot 10^{19}\,\mathrm{cm}^{-3}$ the effective density of states in the Si valence band at 300 K.[16]

Following the explanation given in our previous work,[2] in which similar diodes were investigated by photocurrent spectroscopy, we assume that the energy barrier shown in the inset of Fig. 2 between the Si conduction band (CB) and the PCBM LUMO effectively blocks electron injection into the Si conduction band under forward bias. Instead, the current traverses the organic/inorganic interface as a recombination current between electrons in the PCBM and holes in the p-Si. To describe the balance between the recombination current and the concomitant generation current defining the net current flowing through the device both under forward and reverse bias, we apply the theory of trap assisted recombination of charge carriers given by Shockley and Read,[10] where we treat the LUMO level of PCBM as a trap level of energy E_{LUMO}, capable of capturing and emitting holes (recombination and generation, respectively). For a non-degenerated doped Si, the current density (J_d) through the device is then proportional to the net-rate of recombination, i.e., the difference between the hole capture and emission rates of the LUMO states, which can be calculated assuming detailed balance following Ref. 10:

$$J_d = J_0[p \cdot f_{LUMO} - p_1 \cdot (1 - f_{LUMO})]. \tag{3}$$

Here, p is the total amount of holes in the Si valence band at the interface

$$p = N_V \exp\left(\frac{E_V^{x=0} - E_F^{Si}}{k_B T}\right) \tag{4}$$

and p_1 is the number of holes in the Si valence band at the interface if the Fermi level coincides with E_{LUMO}

$$p_1 = N_V \exp\left(\frac{E_V^{x=0} - E_{LUMO}^{x=0}}{k_B T}\right) = N_V \exp\left(\frac{-\Phi_B}{k_B T}\right). \tag{5}$$

Here, $f_{LUMO} = 1/\{1 + \exp[(E_{LUMO}^{x=0} - E_F^{PCBM})/k_B T]\}$ is the Fermi-Dirac distribution functions of electrons and E_F^{PCBM}, E_F^{Si} are the quasi-Fermi levels on both sides of the interface associated with the top Al/PCBM contact and with the bottom Al/Si contact, respectively. At short circuit conditions, the quasi Fermi levels are equal, however, under an external bias they split by the value of the external bias.

All relevant energy differences appearing in Eq. (3) are obtained from our C-V experiments and the solution of Poisson's equation. Thus, J_0 is the only free parameter available for scaling the ideal generation-recombination (GR) current to the experimental data. For $J_0 = 1 \cdot 10^{-17}\,\mathrm{A \cdot cm}$ and assuming a contact series resistance $R_s = 30\,\Omega/\mathrm{cm}^2$, the red line shown in Fig. 1 is calculated based on the generation-recombination current given by Eqs. (3)–(5). While Fig. 1 shows a reasonably good agreement between experiment and simulation for forward bias, the predicted reverse current density saturating at $J_d^{sat} = -J_0 p_1$ is much smaller than the measured one. Thus, we conclude that the J-V characteristics in reverse direction are dominated by a charge transport via a parallel channel.

For further investigating the origin of the parallel transport channel, the dependence of the reverse current on the temperature was determined. A J-V sweep (−5 V to 2 V) has been recorded every 1 K, while slowly cooling (rate lower than 0.01 K/s) the sample from 340 K to room temperature. For −1.5 V bias, the reverse current as a function of temperature is shown in an Arrhenius plot in Fig. 3. From the slopes, an average activation energy of $E_a = 0.53 \pm 0.02$ eV is obtained from 5 different diodes, where the uncertainty is calculated as the standard deviation. The activation energy is virtually independent of the external bias (see inset of Fig. 3). We want to point out that due to the dominance of parallel transport channel, the activation energy cannot be attributed to the height of the p-Si/PCBM interface barrier.

The trivial explanation for the large reverse current is an ohmic shunt due to pin-holes in the PCBM layer through that the Al directly contacts the p-Si layer or due to defects in the Al-PCBM contact via that holes are injected into the HOMO of PCBM. While such technological defects are definitely present in some of our samples, their dominance in the presented data can be virtually ruled out, since from any batch of processed samples only those with the largest rectification, i.e., with the smallest reverse current were chosen for further

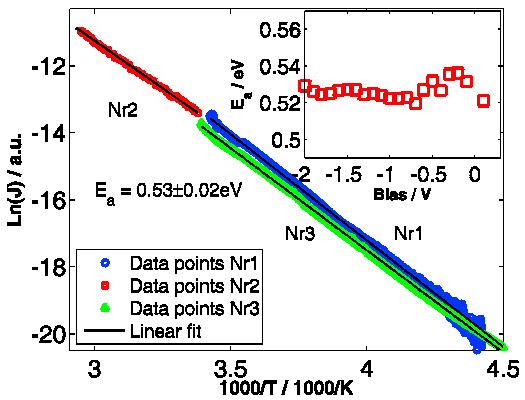

FIG. 3. Arrhenius plot of dark current at reverse bias −1.5 V, for three different samples taken from three different batches fabricated under nominally the same conditions. Inset: Bias dependence of the activation energy.

characterization. These samples show reproducible J-V characteristics, making uncontrolled technical defects extremely unlikely. In addition, the observed activation of the reverse current with temperature cannot be understood based on this trivial model.

On the other hand, it is well known that in Si p-n junctions the net generation-recombination current, which is thermally excited over the Si bandgap throughout the depletion zone is dominating the reverse current by several orders of magnitude as compared to the saturation diffusion current.[15,17,18] The same mechanism has been suggested as origin for the reverse current in organic/inorganic diodes on n-GaAs[19] and p-Si substrates.[20] According to Ref. 15, the generation current depends on the width of the depletion zone w_{Si} and the intrinsic carrier density n_i of the substrate semiconductor. For large enough reverse biases for which $p < n_i$ in the dominant part of a depletion region, the space charge region generation current density can be approximated by: $J_{gen}^{rev} = |q| n_i w_{Si}/\tau_e$, where τ_e is the effective lifetime of the thermally generated minority carriers in the substrate semiconductor.

Due to the proportionality of J_{gen}^{rev} to n_i, its thermal activation depends exponentially on $E_g/2k_BT$, where E_g is the bandgap of the substrate semiconductor. The activation energy obtained from Fig. 3 (0.53 ± 0.02 eV) is in excellent agreement with the value that one would expect based on the bandgap of the Si substrate. Also, the order of magnitude of the measured reverse current density, shown by the black line in Fig. 1, is in line with this interpretation, as evidenced by evaluating J_{gen}^{rev} using $\tau_e \approx 0.1\,\mu$s as typical value for Si.[17]. However, since w_{Si} is proportional to square root of external voltage, the same dependence is expected for the generation current. The deviation from the square root dependence for $V_{bias} < -2\,V$ shown in the inset of Fig. 1 could be tentatively assigned to the additional parallel channel associated with the tunneling of electrons through a triangular barrier (Fowler-Nordheim tunneling[12]) formed at the interface.

In a previous publication,[2] it was shown that similar PCBM/p-silicon diodes show a photo-response for photons with energy $\hbar\omega \geq \Phi_B \simeq 0.55$ eV, which is also observed for the diodes investigated in this work. The results for the energy level structure across the p-Si/PCBM interface obtained here by electrical methods are in full agreement with the onset energy of the photocurrent as reported in Ref. 2, confirming the previously presented model for photocurrent generation at the interface due to an enhancement of the hole capture rate of the PCBM LUMO level by photon absorption.

IV. CONCLUSIONS

A novel comprehensive model for the operation of p-Si/PCBM hybrid diode, based on an interface generation-recombination current, was proposed. The band diagram based on energy values obtained experimentally from C-V measurement was presented. The energy difference between VB of p-Si and LUMO of PCBM is identified as interface barrier height and defines the onset of the spectrally resolved photocurrent reported previously.[2] Based on the detailed understanding of the diode operation principle, further improvements of the device with respect to its application as infrared photodetector compatible with standard Si technology[21] as well as the development of photodetectors based on alternative organic semiconductors becomes possible.

ACKNOWLEDGMENTS

This work was supported by the Oesterreichische Forschungsfoerderungsgesellschaft (FFG Project Nos. 818046 and 834913). The authors would like to thank Konarka Austria for the support of this work.

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